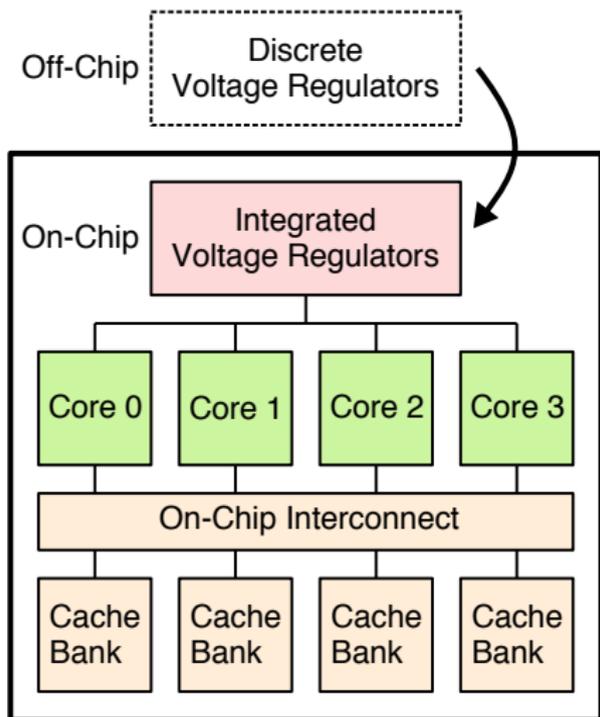# Enabling Realistic
Fine-Grain Voltage Scaling with
Reconfigurable Power Distribution Networks

Waclaw Godycki, Christopher Torng, Ivan Bukreyev
Alyssa Apsel, Christopher Batten

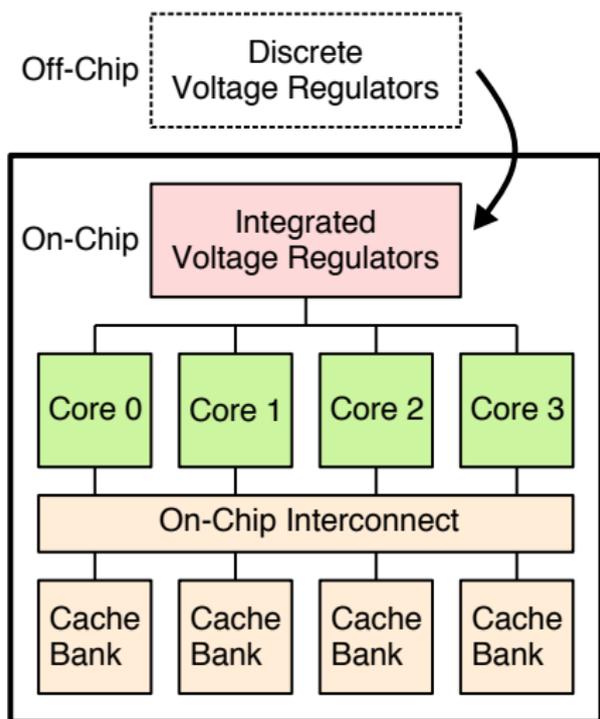School of Electrical and Computer Engineering
Cornell University

Motivation: Integrated Voltage Regulation (IVR)

Key Benefit of IVR

▶ Reduced System Cost

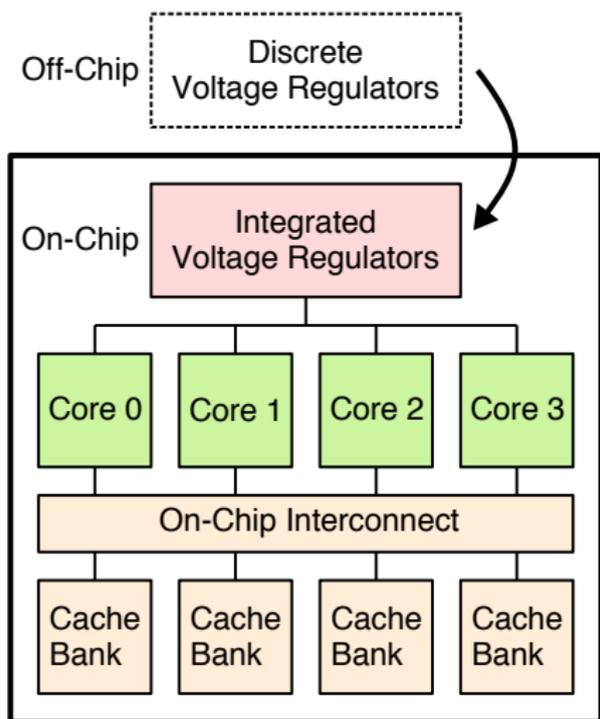# **Motivation: Integrated Voltage Regulation (IVR)**

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Challenges of IVR

▶ Integrated energy-storage elements have low energy densities
▶ Low switching speeds with high parasitic losses

Motivation: Integrated Voltage Regulation (IVR)

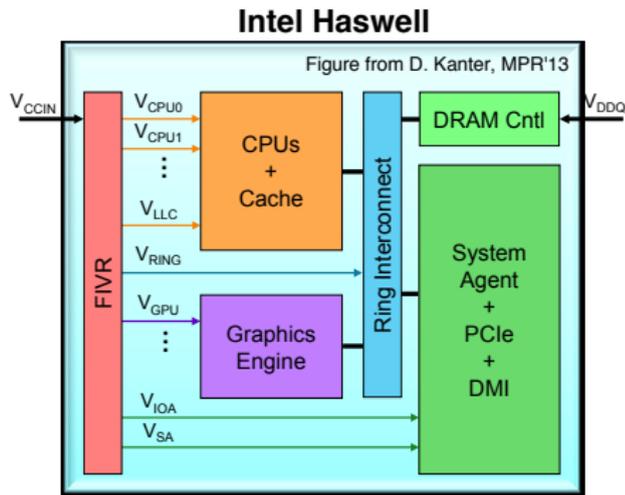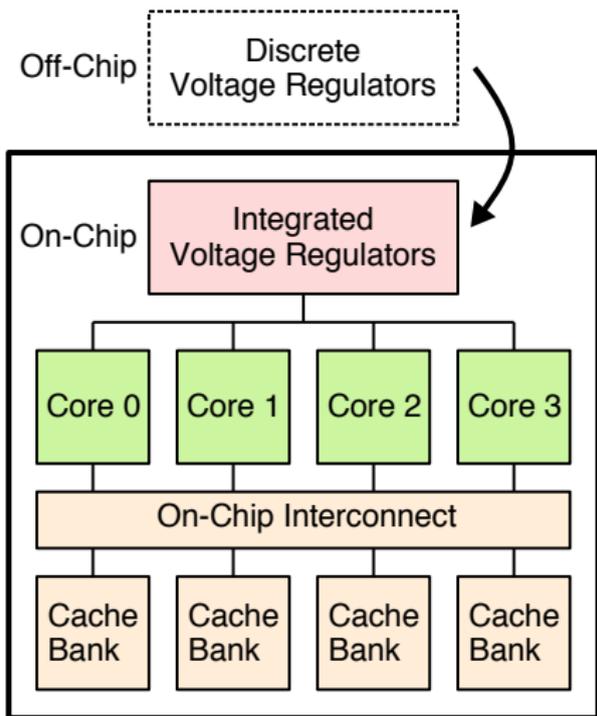**Key Benefit of IVR**

▶ Reduced System Cost

Challenges of IVR

▶ Integrated energy-storage elements have low energy densities
▶ Low switching speeds with high parasitic losses

A New Era of IVR

▶ Energy storage elements have slightly improved energy densities
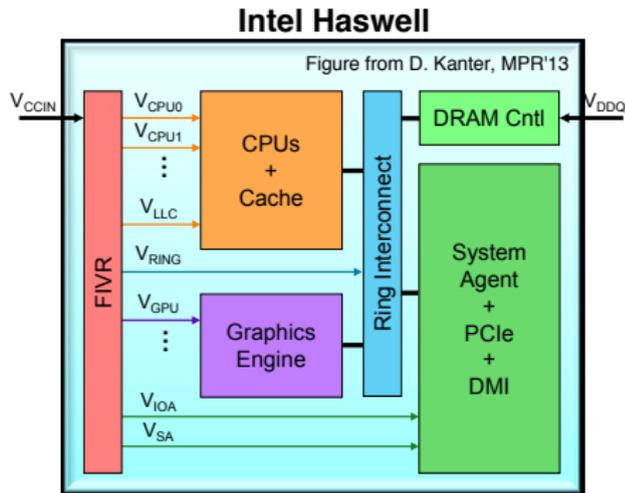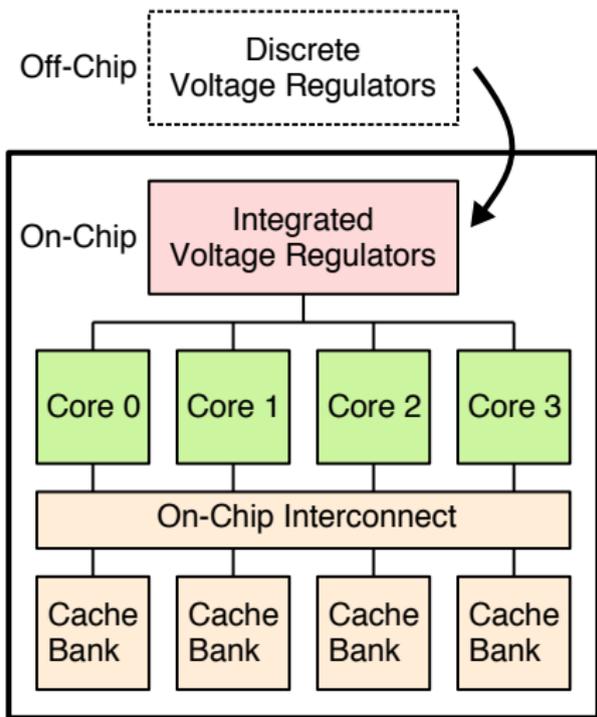▶ Faster switches with low parasitic losses

Motivation: Integrated Voltage Regulation (IVR)

Intel Haswell

Figure from D. Kanter, MPR'13

"Fully" Integrated Voltage Regulator (FIVR)

Intel Haswell integrates the
voltage control loop circuitry *on-die*
with inductors *in-package*.

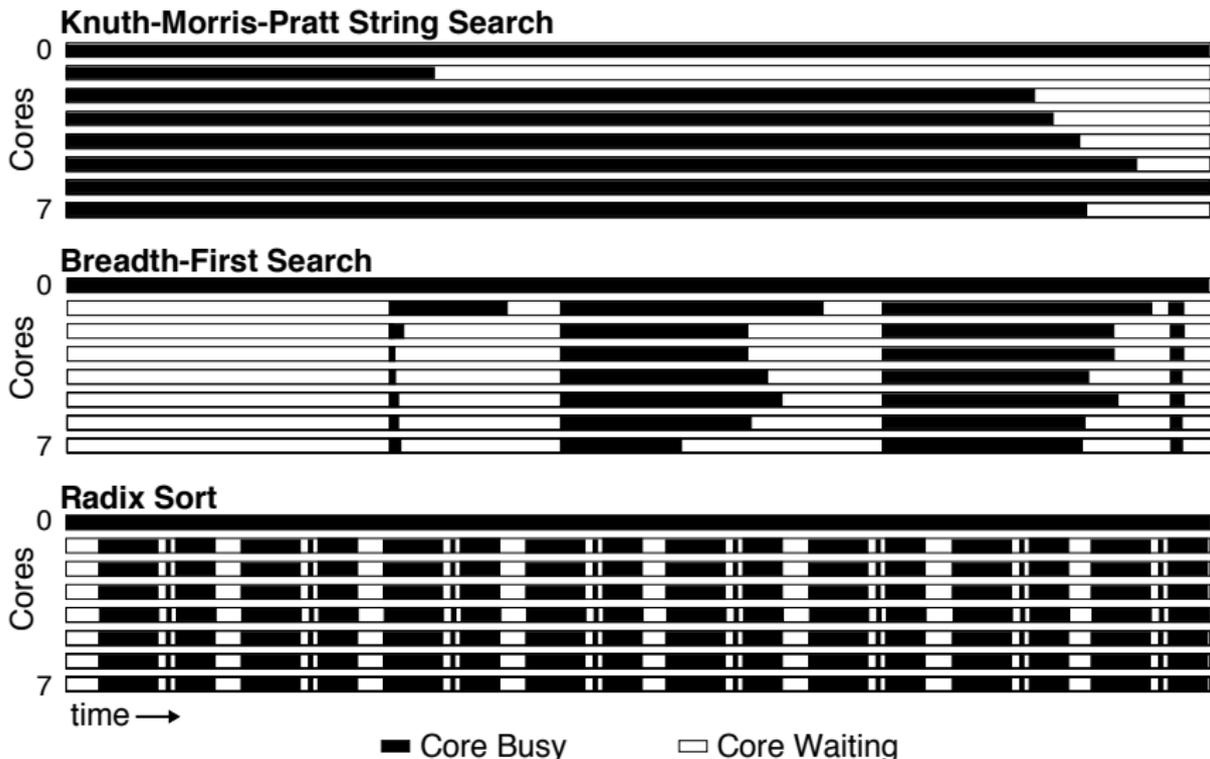# **Motivation: Integrated Voltage Regulation (IVR)**

Intel Haswell

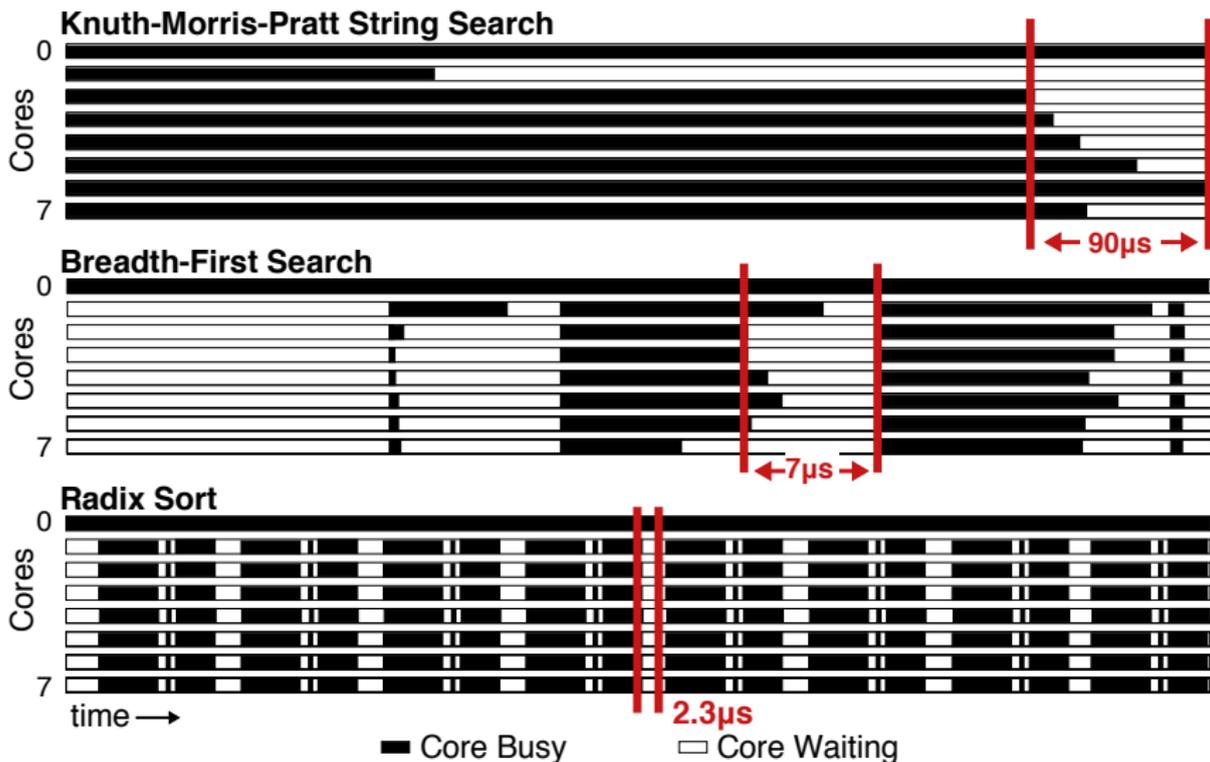Figure from D. Kanter, MPR'13

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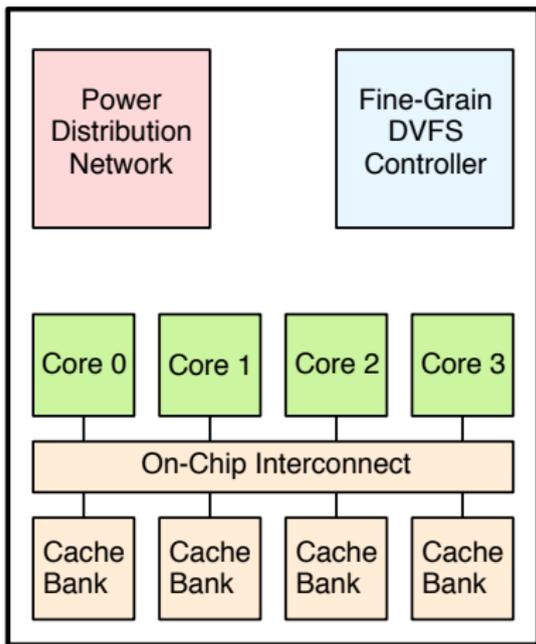**Potential for Fine-Grain Voltage Scaling**

Motivation: Fine-Grain Voltage Scaling Opportunities

Knuth-Morris-Pratt String Search

Breadth-First Search

Radix Sort

time →

■ Core Busy   □ Core Waiting

Motivation: Fine-Grain Voltage Scaling Opportunities

Knuth-Morris-Pratt String Search

← **90μs** →

Breadth-First Search

←**7μs**→

Radix Sort

time →

■ Core Busy   ☐ Core Waiting

2.3μs

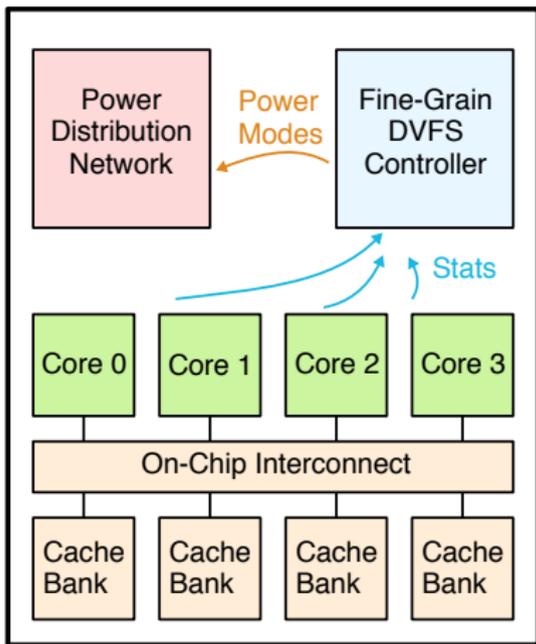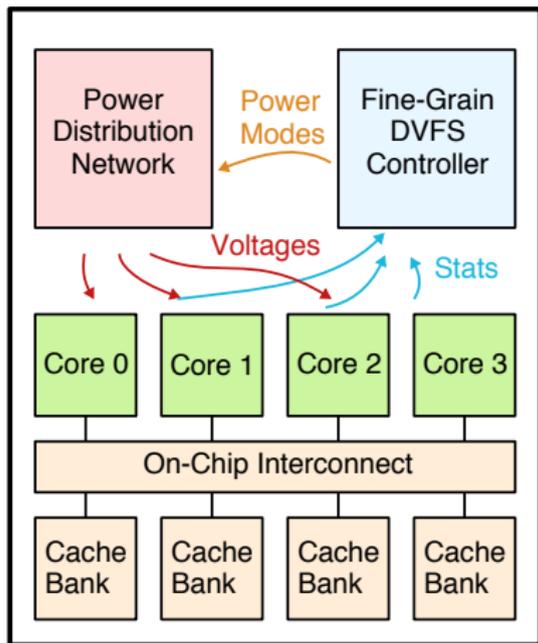# **Enabling Realistic Fine-Grain Voltage Scaling**

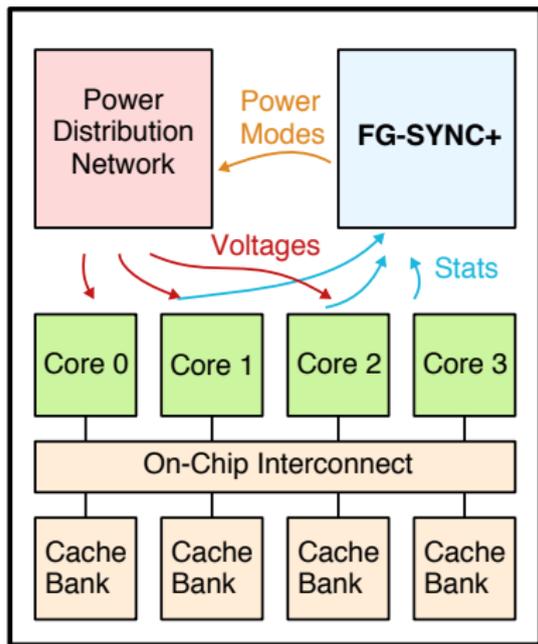# Enabling Realistic Fine-Grain Voltage Scaling
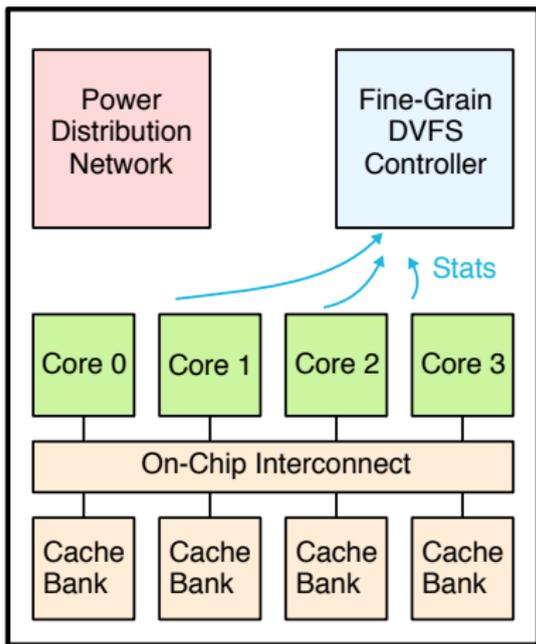
Enabling Realistic Fine-Grain Voltage Scaling

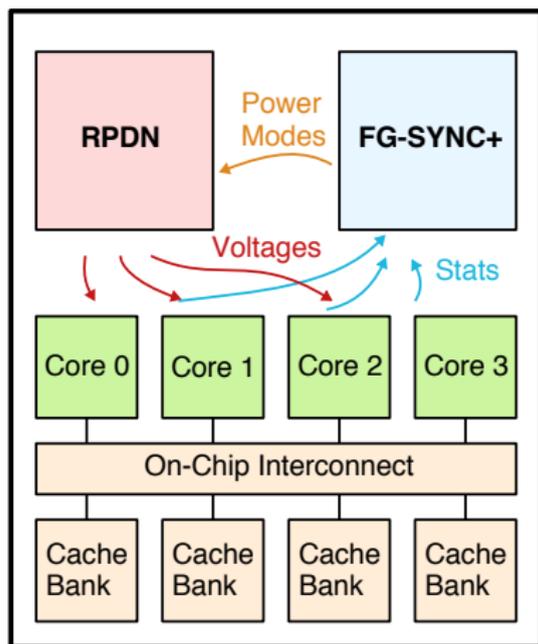# Enabling Realistic Fine-Grain Voltage Scaling

Enabling Realistic Fine-Grain Voltage Scaling

FGVS Architecture: FG-SYNC+

Use lightweight software hints and lookup tables derived offline to enable fast multi-level voltage configuration

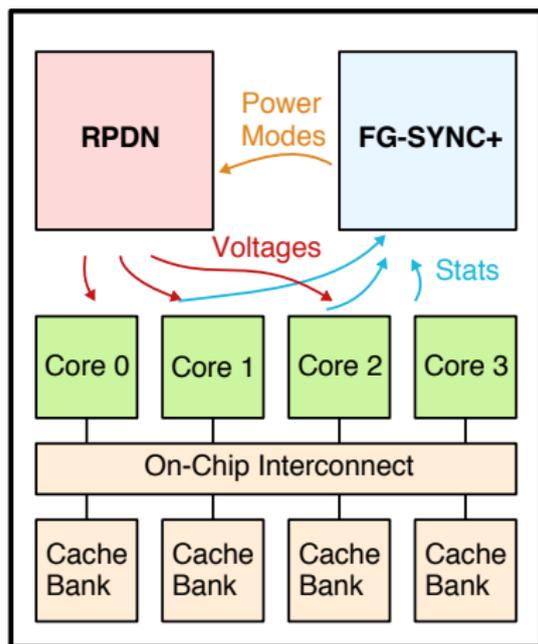# **Enabling Realistic Fine-Grain Voltage Scaling**
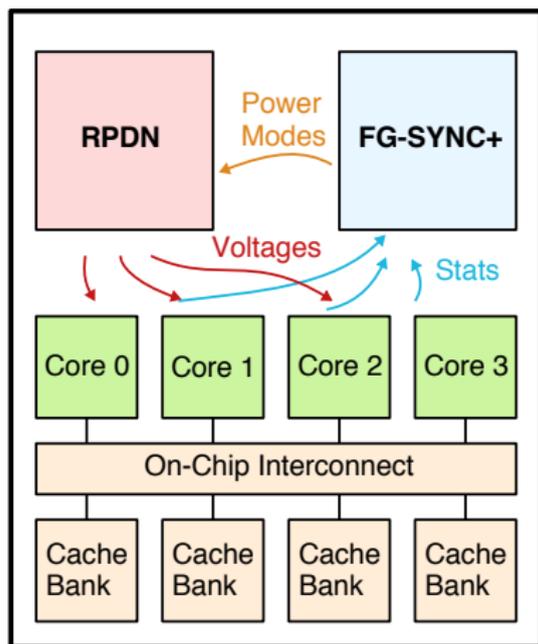

FGVS Architecture: FG-SYNC+

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FGVS Circuits: RPDN

Enable sprinting cores to dynamically borrow energy storage from resting cores

Enabling Realistic Fine-Grain Voltage Scaling

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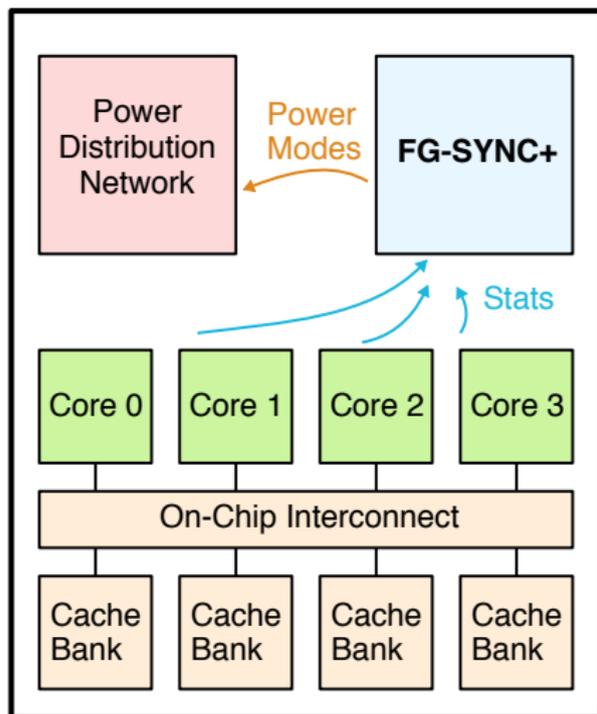
Methodology and Evaluation

Enabling Realistic Fine-Grain Voltage Scaling

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Methodology and Evaluation

Architecture and Circuits Co-Design Approach
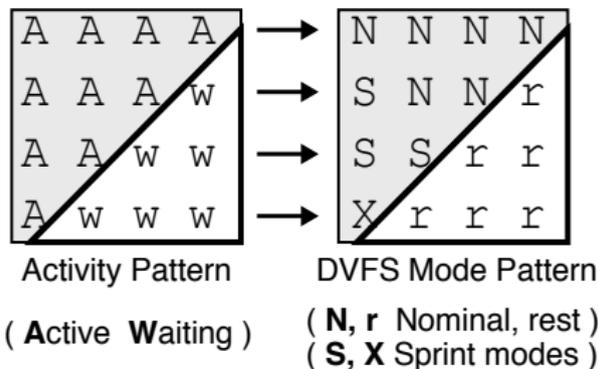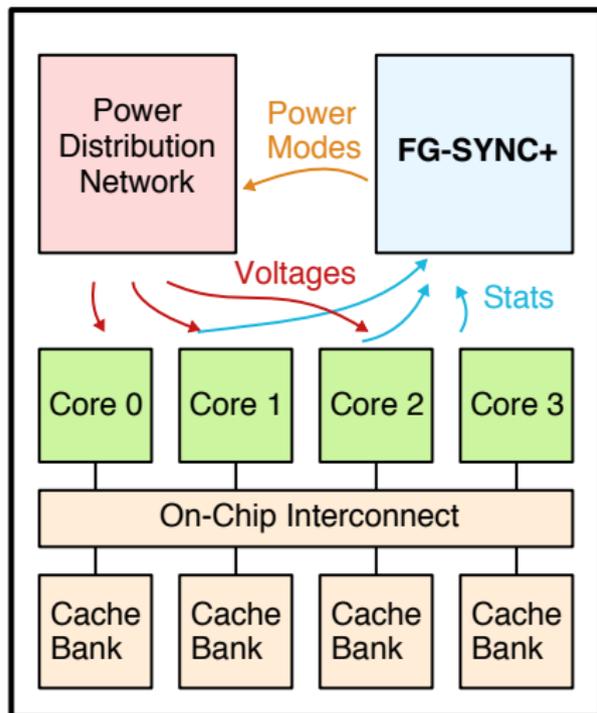
Fine-Grain Synchronization Controller (FG-SYNC+)
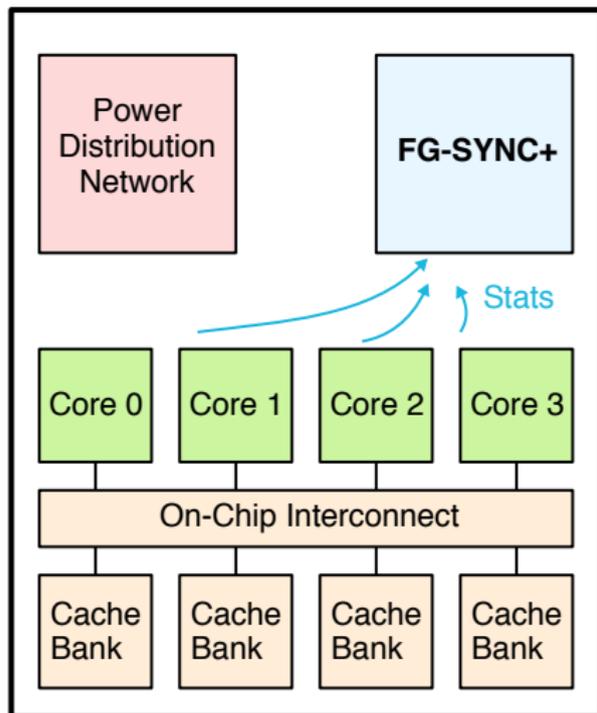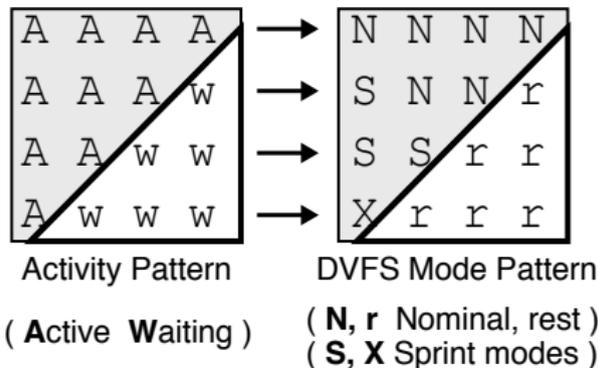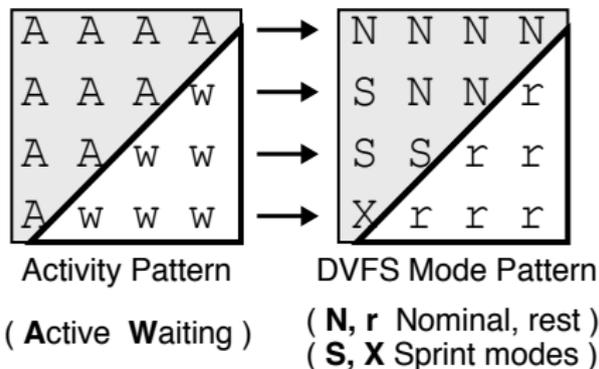


```
parallel_for(int i=0; i<N; n++){
    Before Start: Work Left Hint
    Loop Start: Activity Hint -- busy
    < loop body >
    Loop Ends: Activity Hint -- waiting
}
```
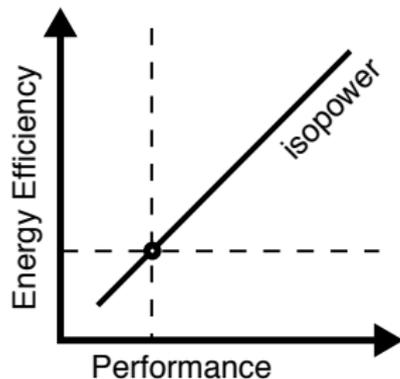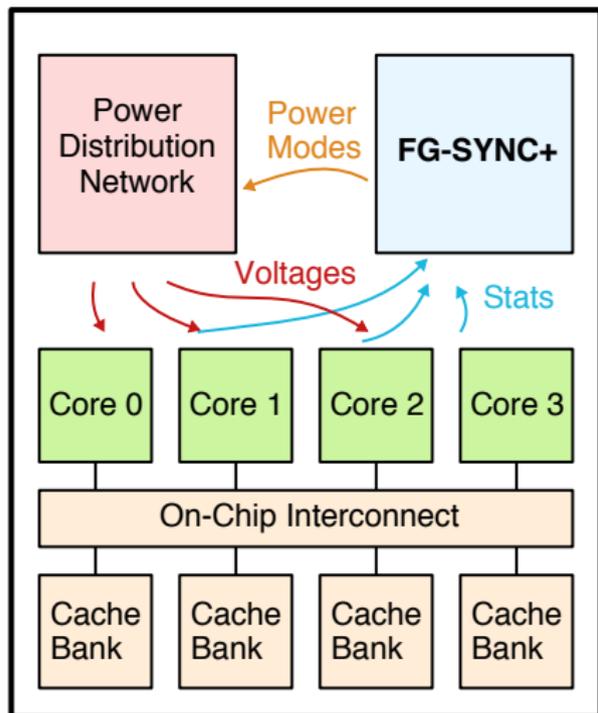
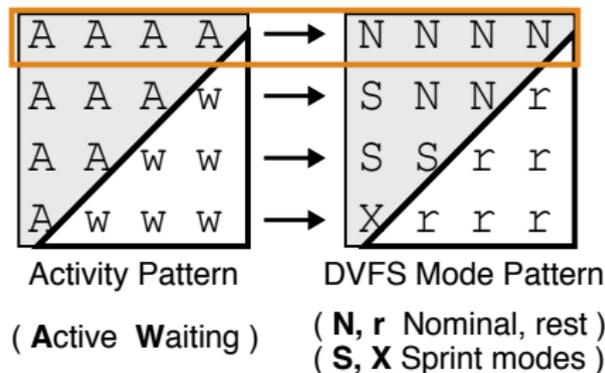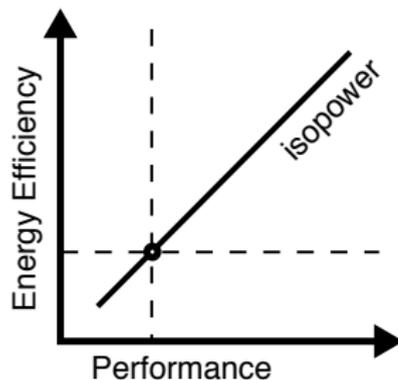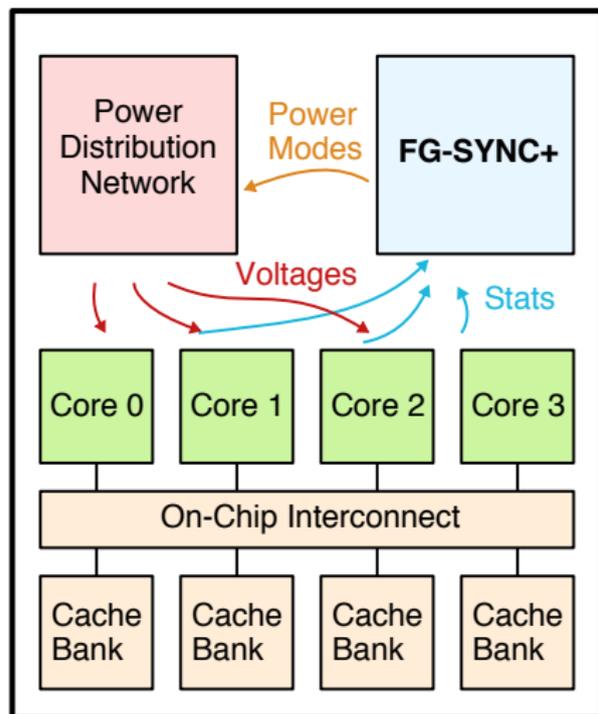# Fine-Grain Synchronization Controller (FG-SYNC+)


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Activity Pattern   DVFS Mode Pattern

(**A**ctive **W**aiting)   (**N, r** Nominal, rest)
                          (**S, X** Sprint modes)

Fine-Grain Synchronization Controller (FG-SYNC+)


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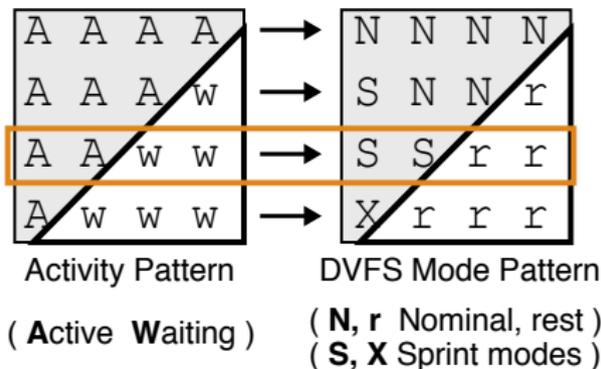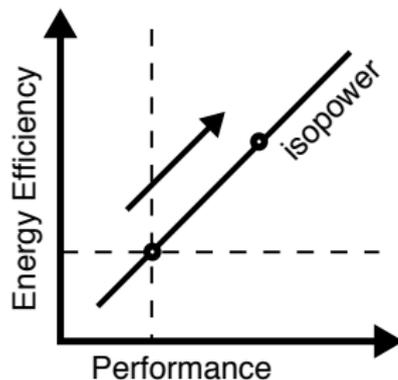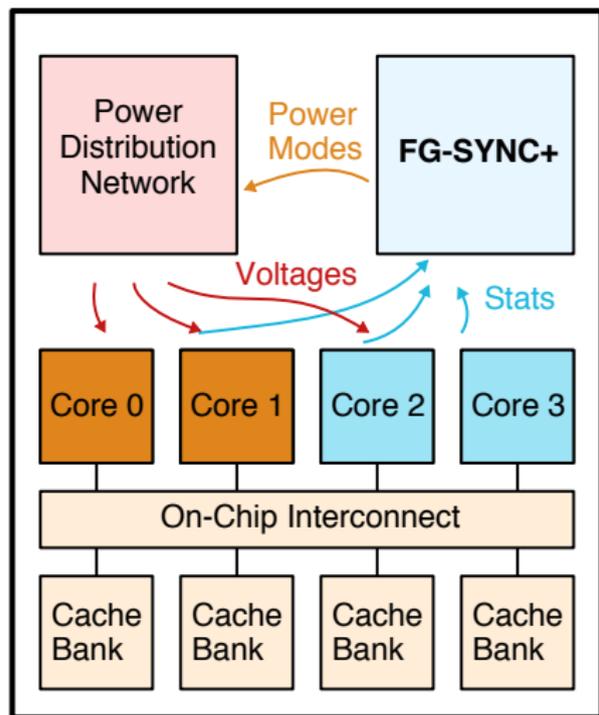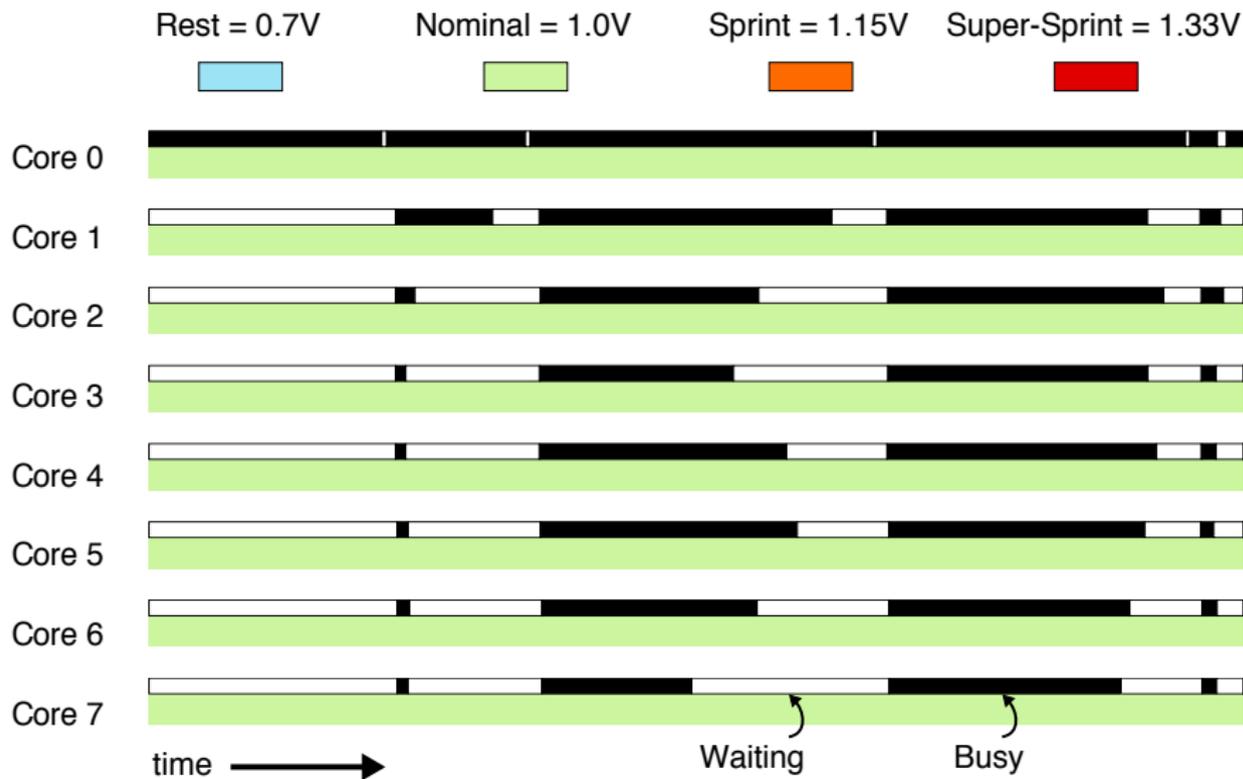
Activity Pattern

(**A**ctive **W**aiting)

DVFS Mode Pattern

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Fine-Grain Synchronization Controller (FG-SYNC+)

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Fine-Grain Synchronization Controller (FG-SYNC+)

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Fine-Grain Synchronization Controller (FG-SYNC+)

Activity Pattern → DVFS Mode Pattern

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Ideal Fine-Grain Voltage Scaling: Breadth-First Search

Rest = 0.7V   Nominal = 1.0V   Sprint = 1.15V   Super-Sprint = 1.33V

Core 0
Core 1
Core 2
Core 3
Core 4
Core 5
Core 6
Core 7

time ⟶   Waiting   Busy

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Execution Time Reduced by 24%

Ideal FGVS Level Space Time

time ⟶

Waiting   Busy

Non-Ideal FGVS: Different Levels

2-Level Controllers

No FGVS

Non-Ideal FGVS: Different Levels

2-Level Controllers

Non-Ideal FGVS: Different Levels

2-Level Controllers

Non-Ideal FGVS: Different Levels

2-Level Controllers

Non-Ideal FGVS: Different Levels
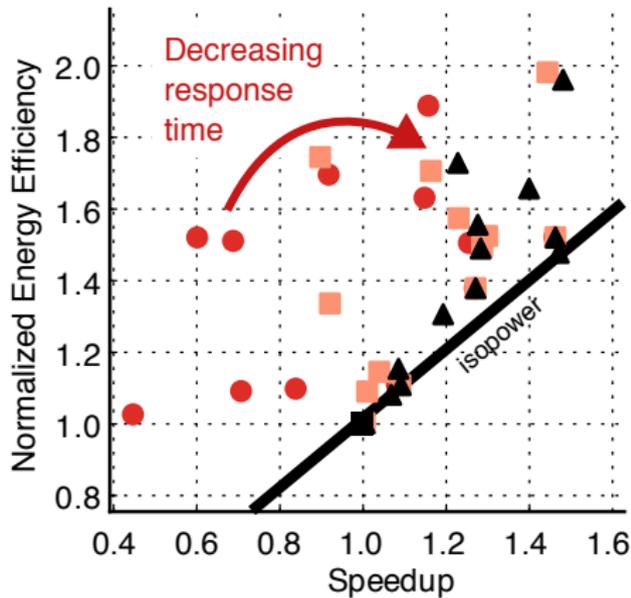

2-Level Controllers

3-Level vs 4-Level Controllers

Increasing sprinting levels

isopower

No FGVS   r / N
N / S   N / X

No FGVS   r / N / S
r / N / X   r / N / S / X
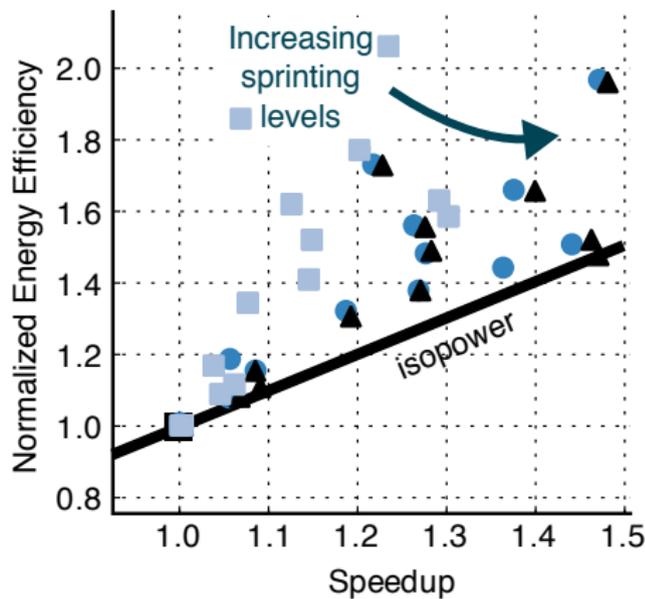
# Non-Ideal FGVS: Space and Time
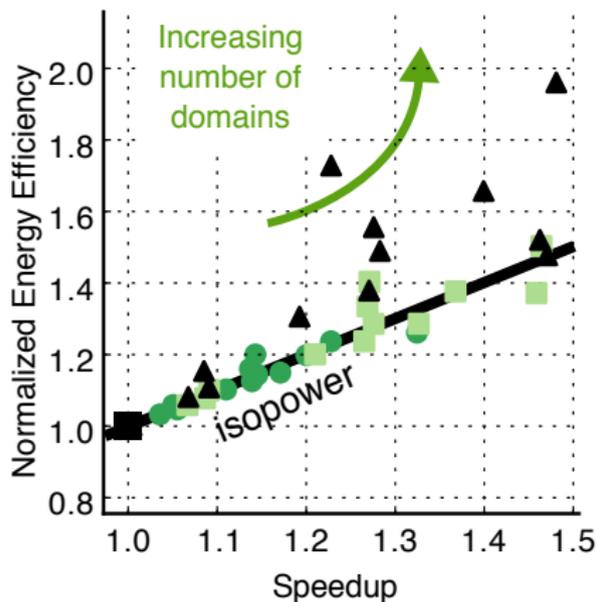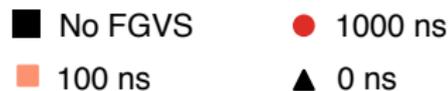
FG-SYNC+: Summary of FGVS Potential

Exploiting fine-grain voltage scaling requires:

▶ **FGVS in Level**: at least three levels and four levels results in additional benefits

▶ **FGVS in Space**: per-core voltage control

▶ **FGVS in Time**: voltage settling response times of 100 ns or faster

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How do we design a power distribution network that can enable fine-grain voltage scaling?

FG-SYNC+: Summary of FGVS Potential

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Architecture and Circuits Co-Design Approach

Talk Outline
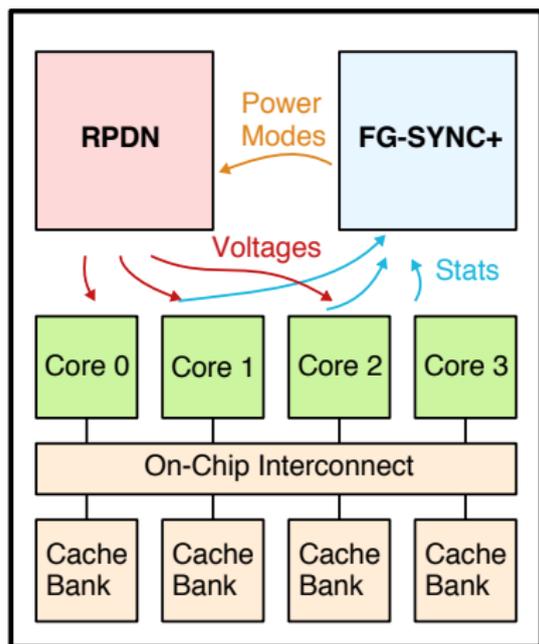
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Methodology and Evaluation

Architecture and Circuits Co-Design Approach

PDN: Basic Regulators

The three primary types of step-down voltage regulators are linear regulators, inductor-based switching regulators (buck), and capacitor-based switching regulators.
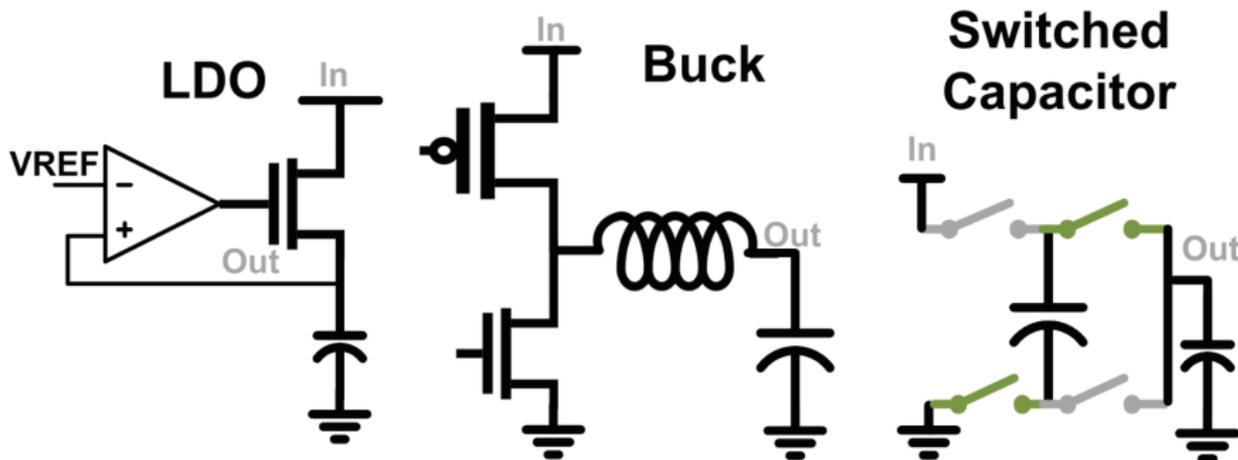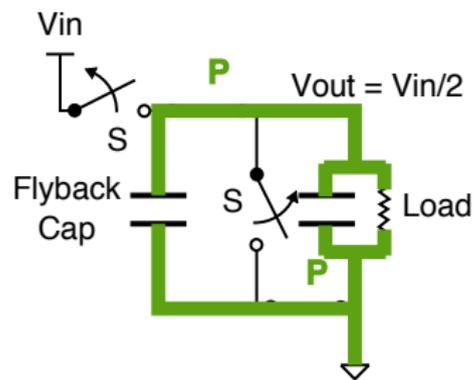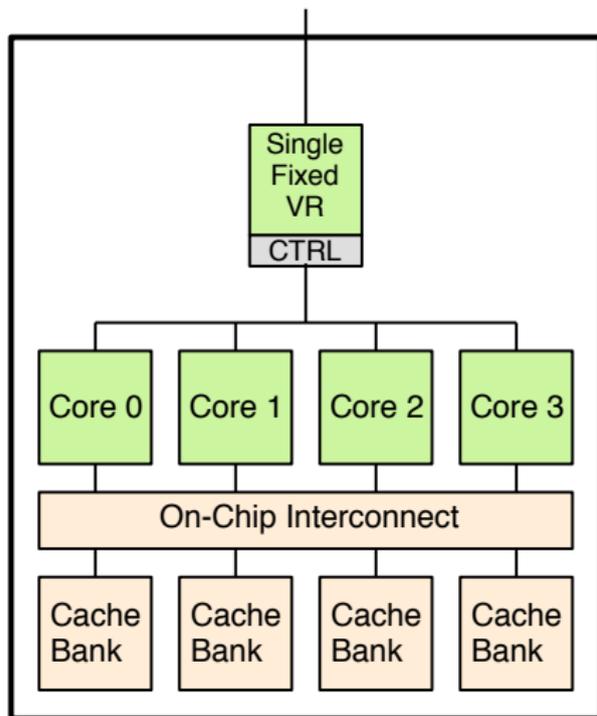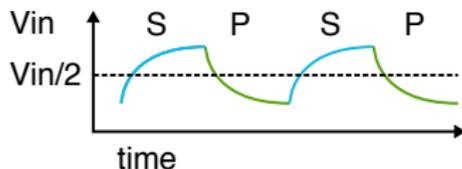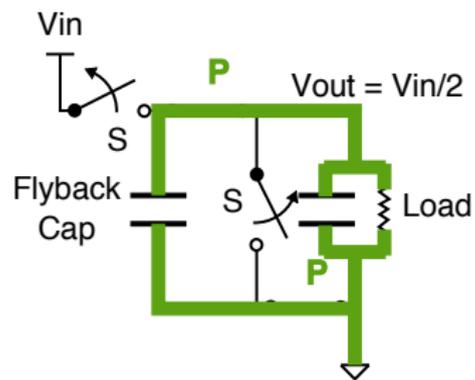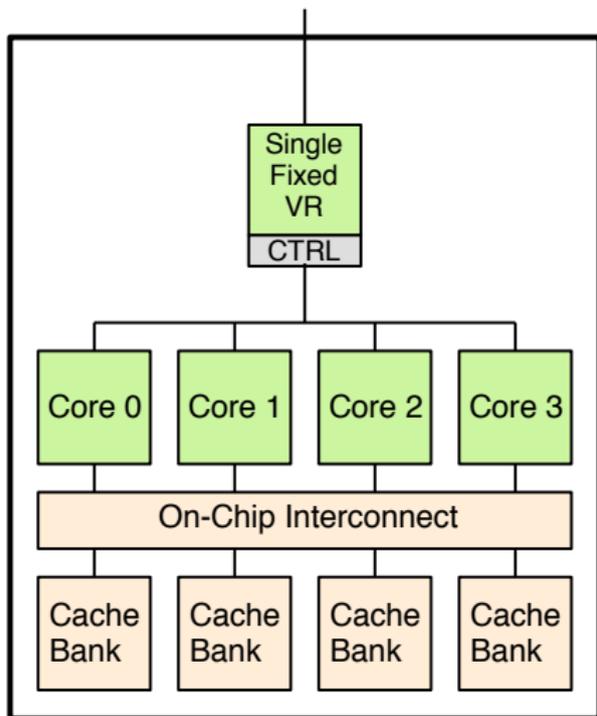
A Simple On-Chip Power Distribution Network
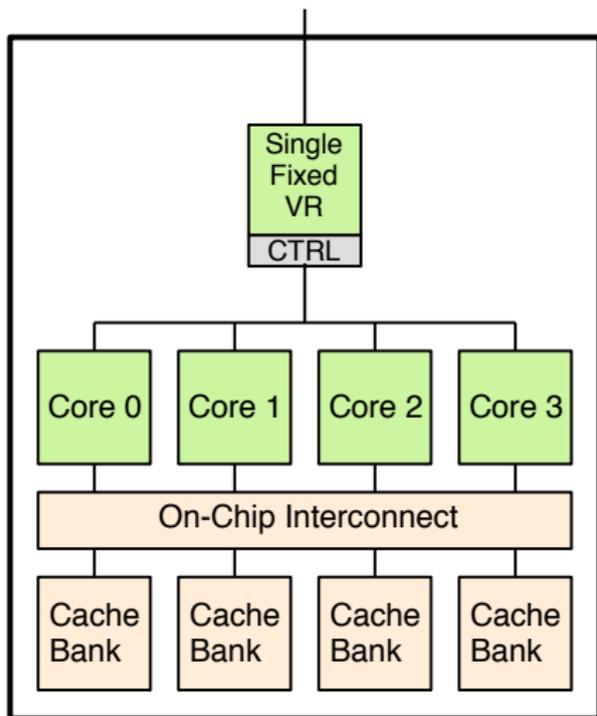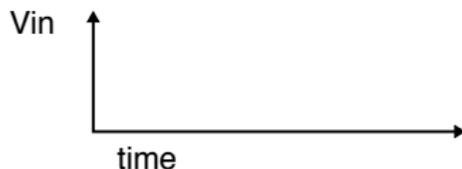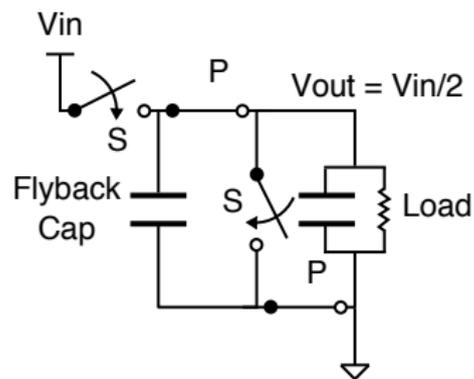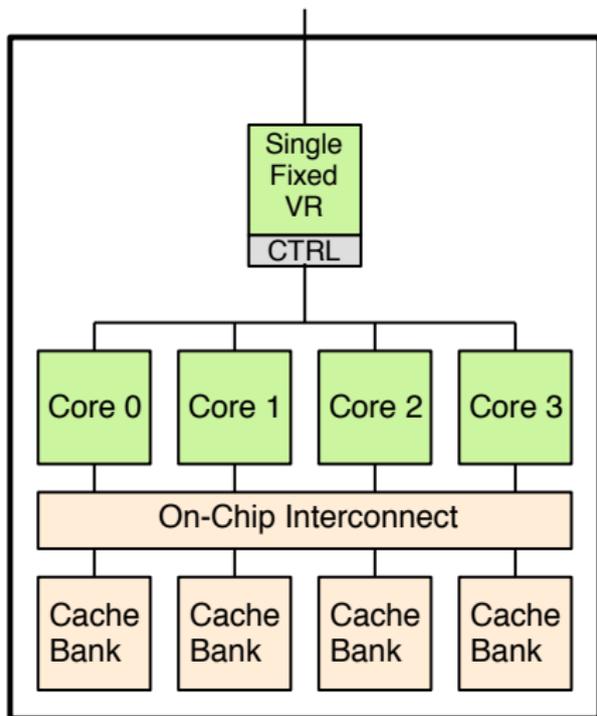
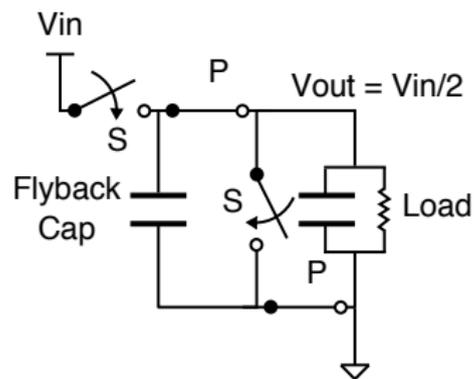# A Simple On-Chip Power Distribution Network

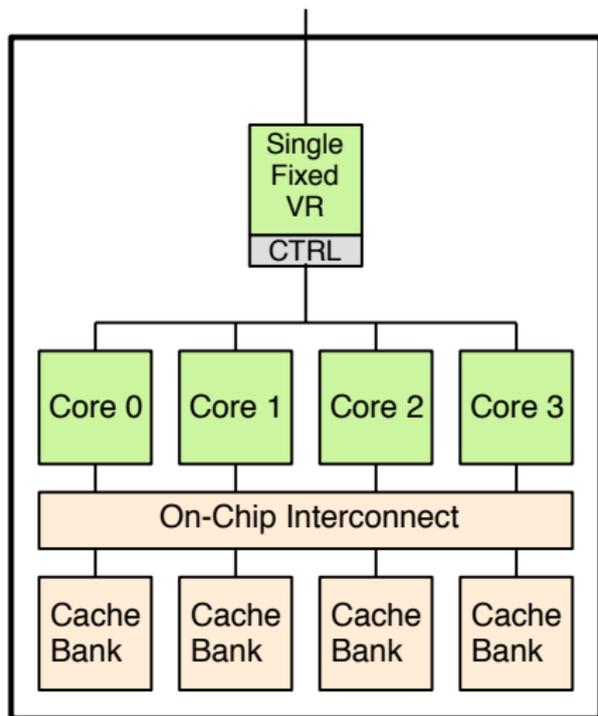# A Simple On-Chip Power Distribution Network
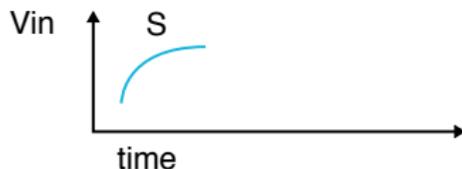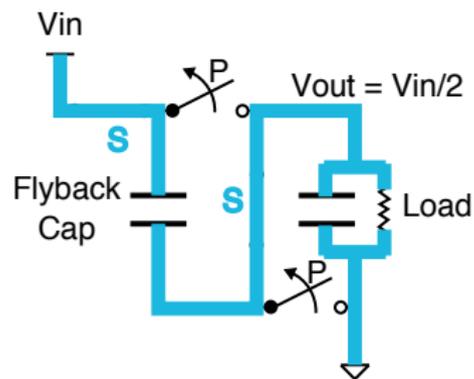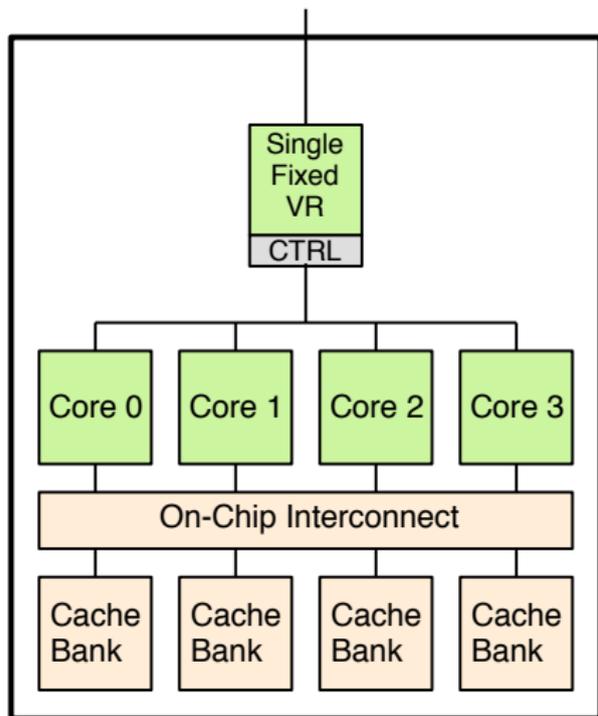
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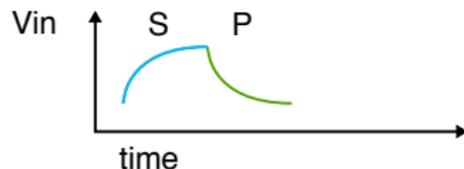
A Simple On-Chip Power Distribution Network

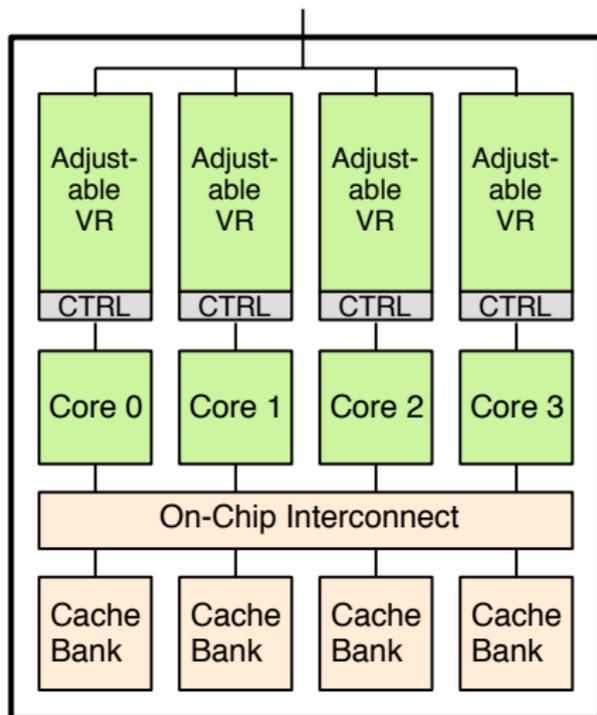# **A Simple On-Chip Power Distribution Network**

How to design sophisticated control circuitry?
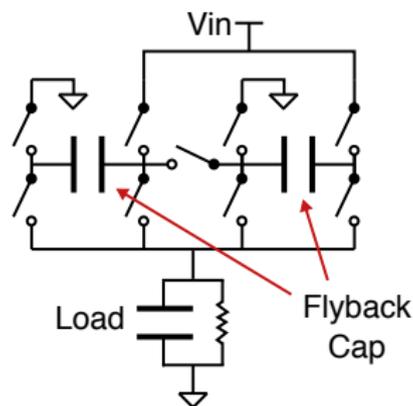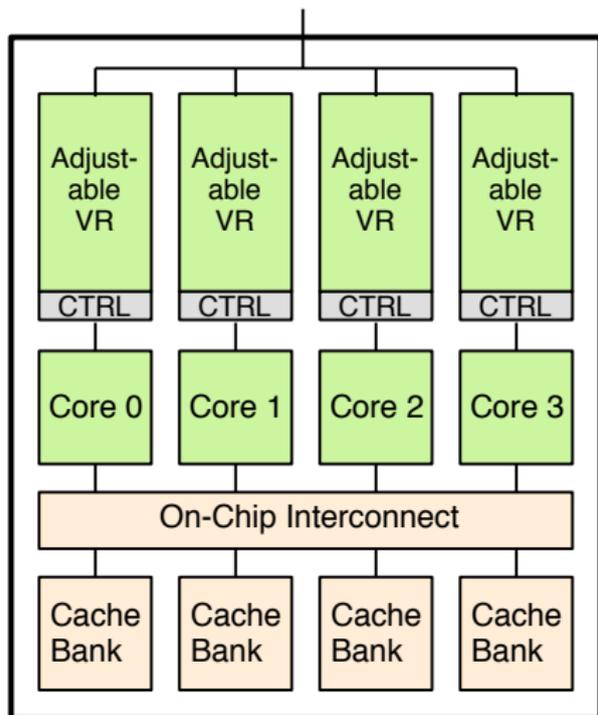
How to use multiple phases to reduce ripple?

How to size the energy storage?

How to choose the switch-to-cap area ratio?

MAVR: Multiple Adjustable Voltage Regulators

MAVR: Multiple Adjustable Voltage Regulators

MAVR: Multiple Adjustable Voltage Regulators

How to design sophisticated control circuitry?

How to use multiple phases to reduce ripple?

How to size the energy storage?

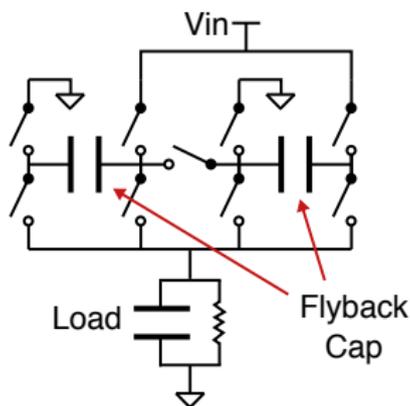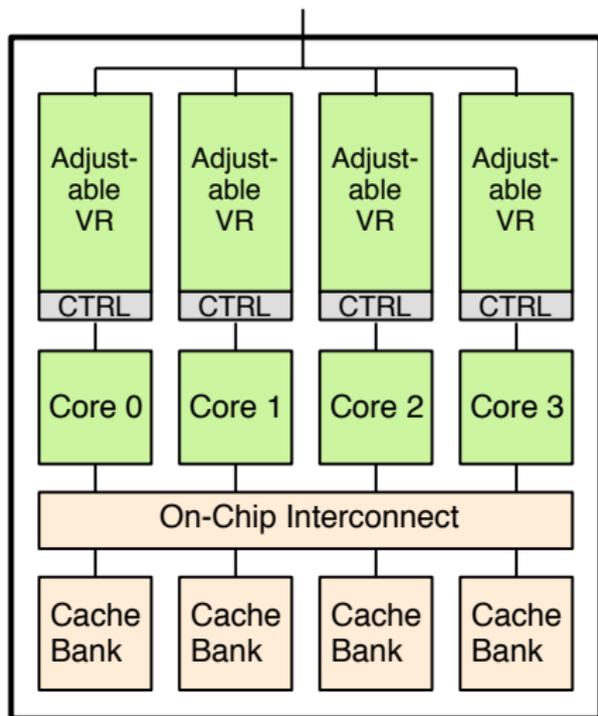How to choose the switch-to-cap area ratio?

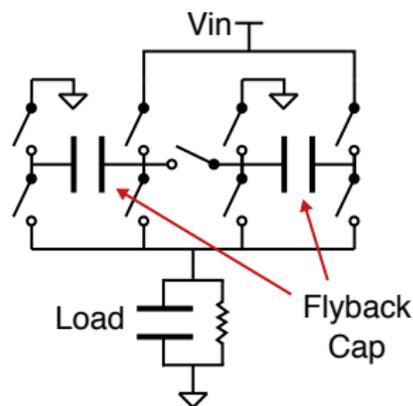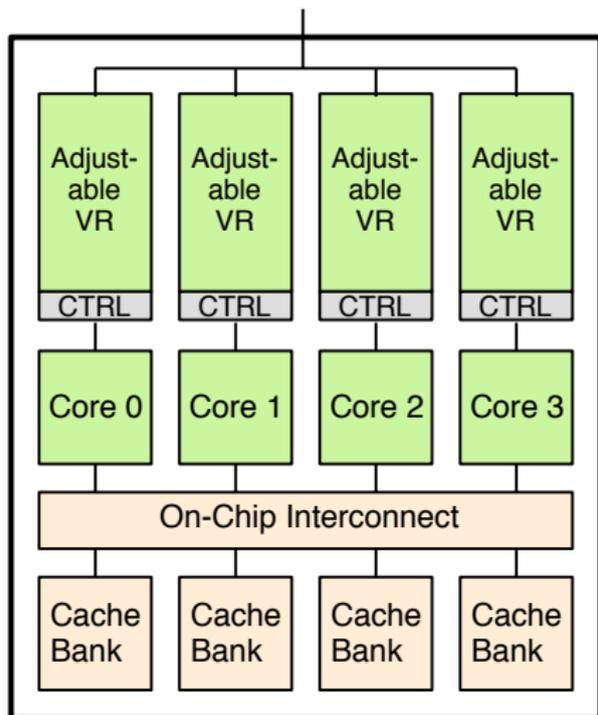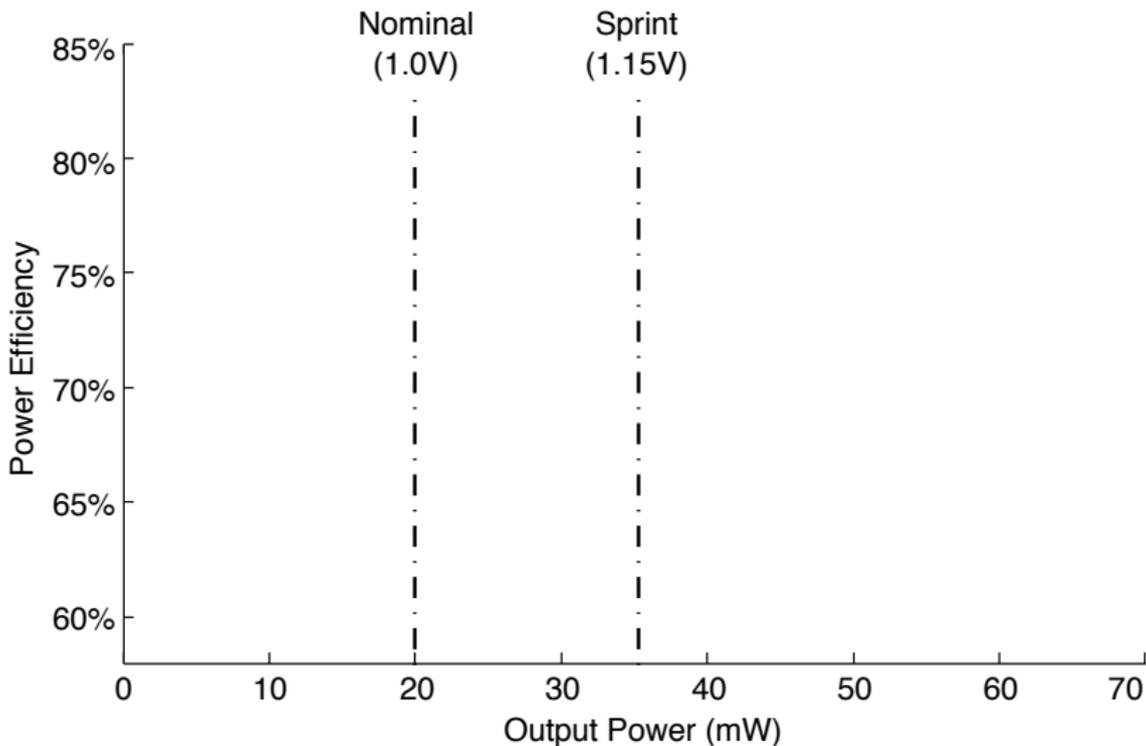# MAVR: Multiple Adjustable Voltage Regulators

How to design sophisticated control circuitry?
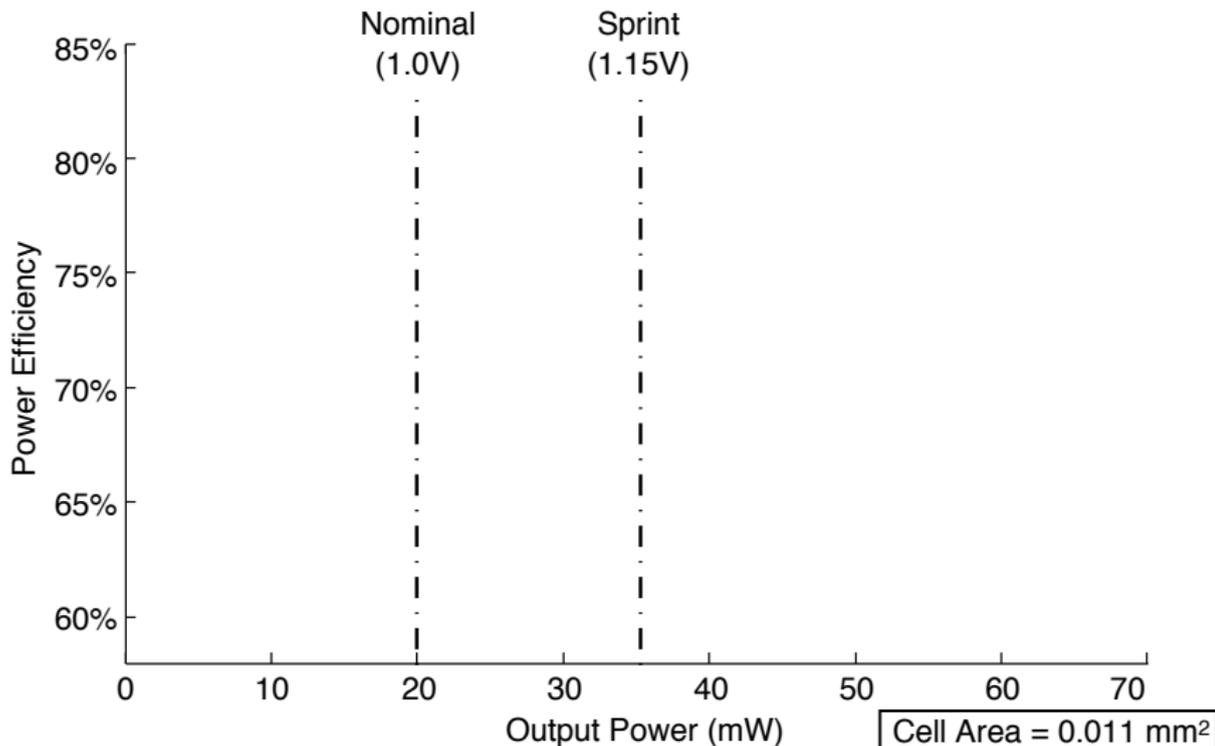
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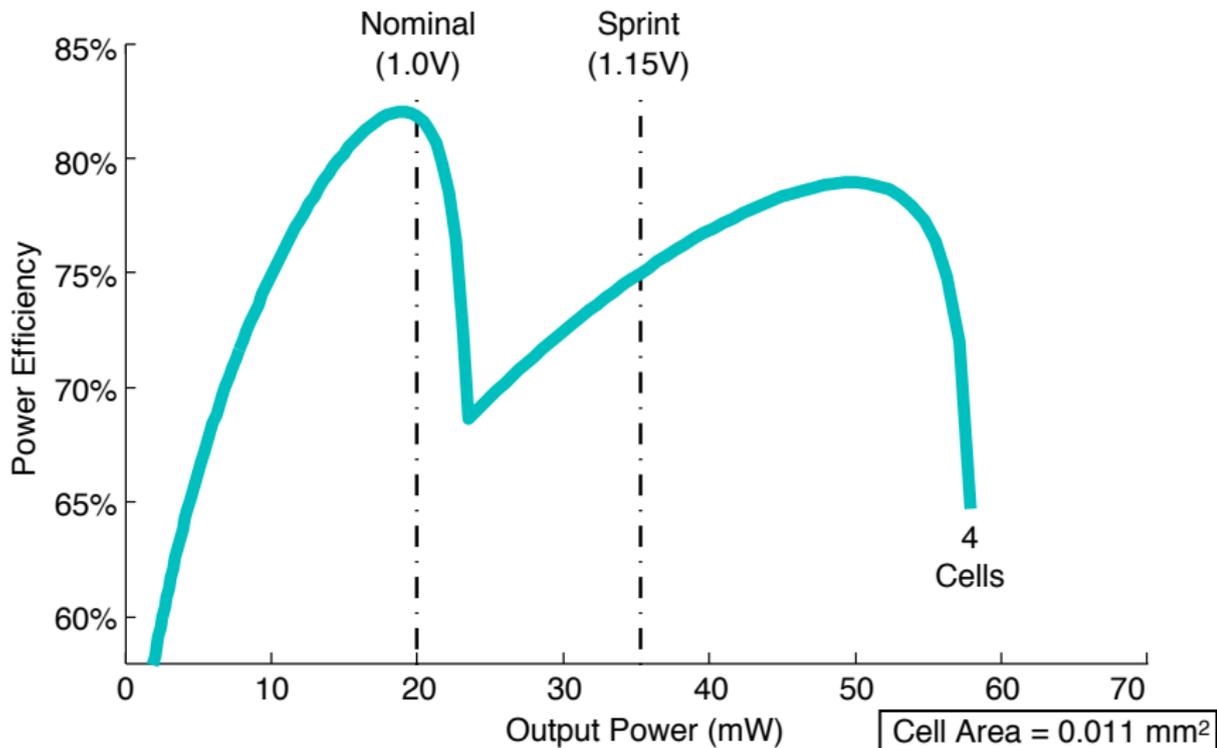
How to choose the switch-to-cap area ratio?

MAVR: Per-Core Regulator Sizing Study
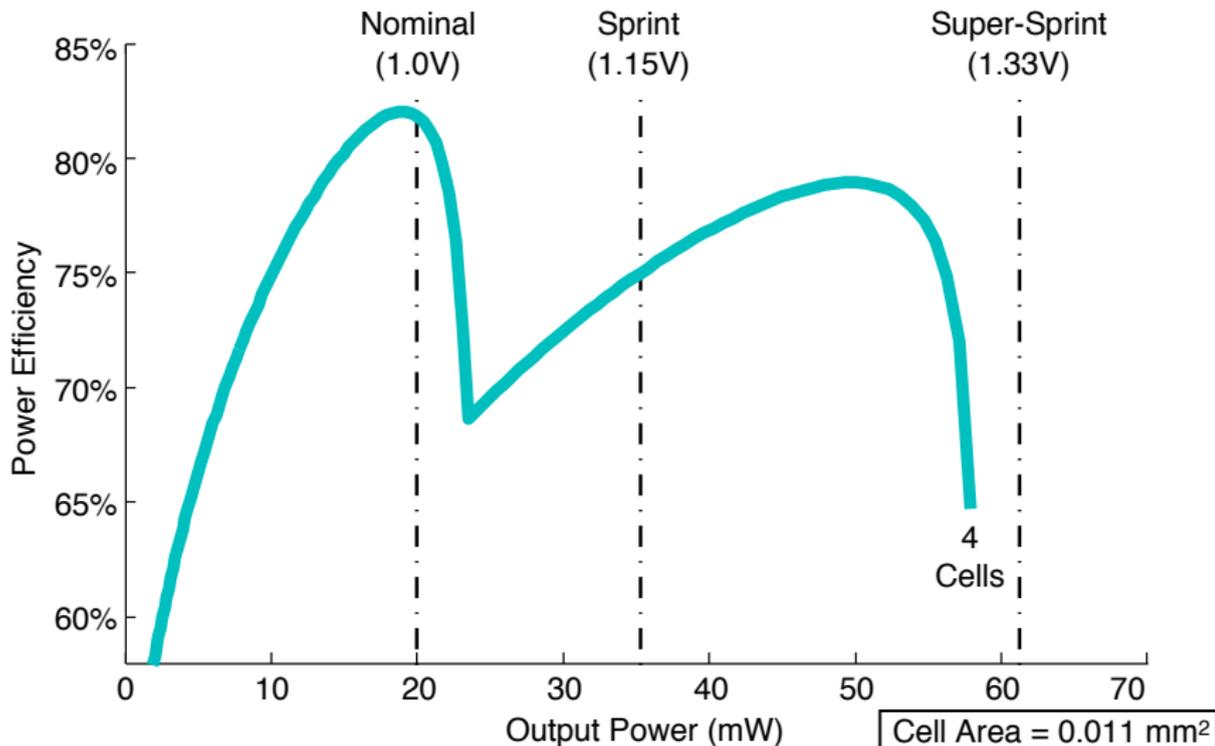
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MAVR: Per-Core Regulator Sizing Study

Cell Area = 0.011 mm^2
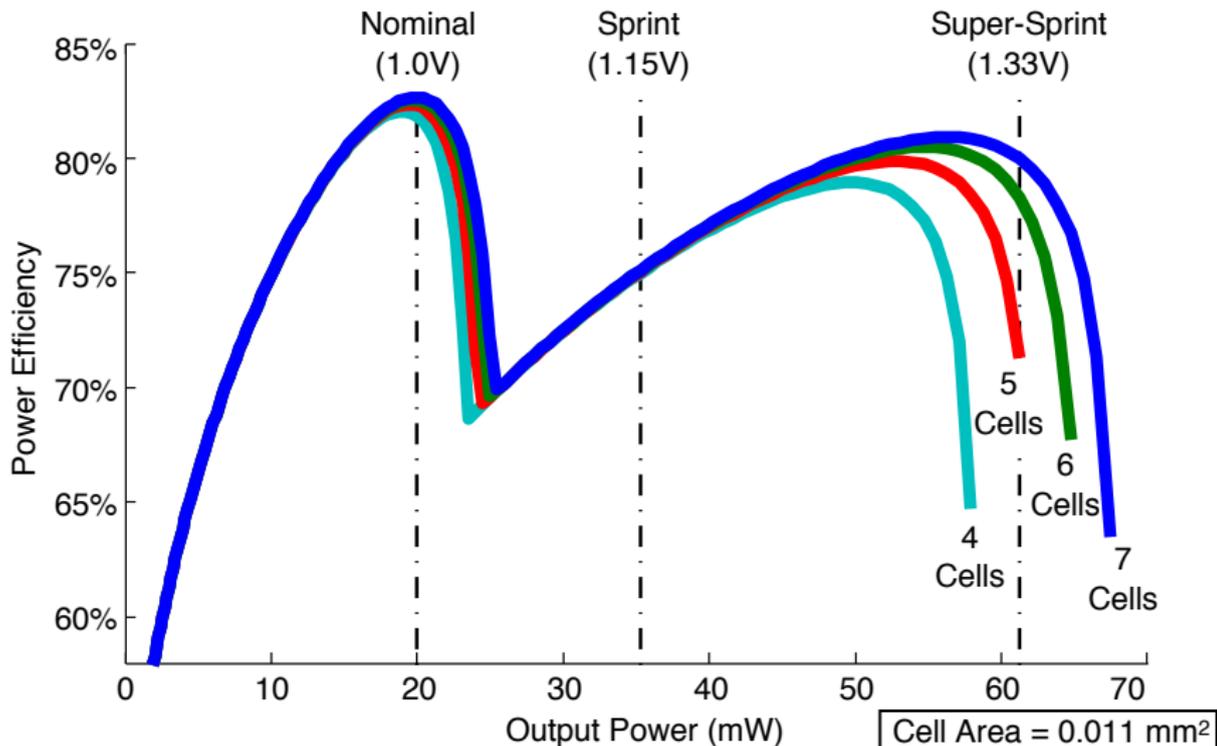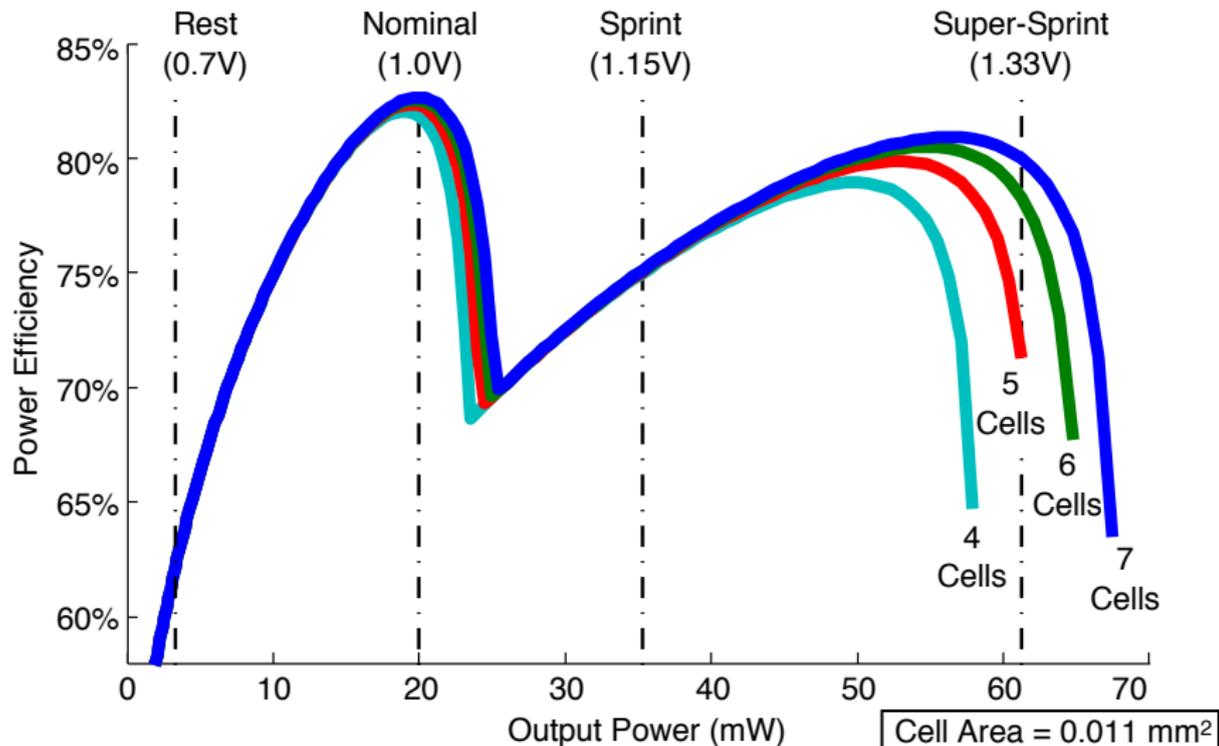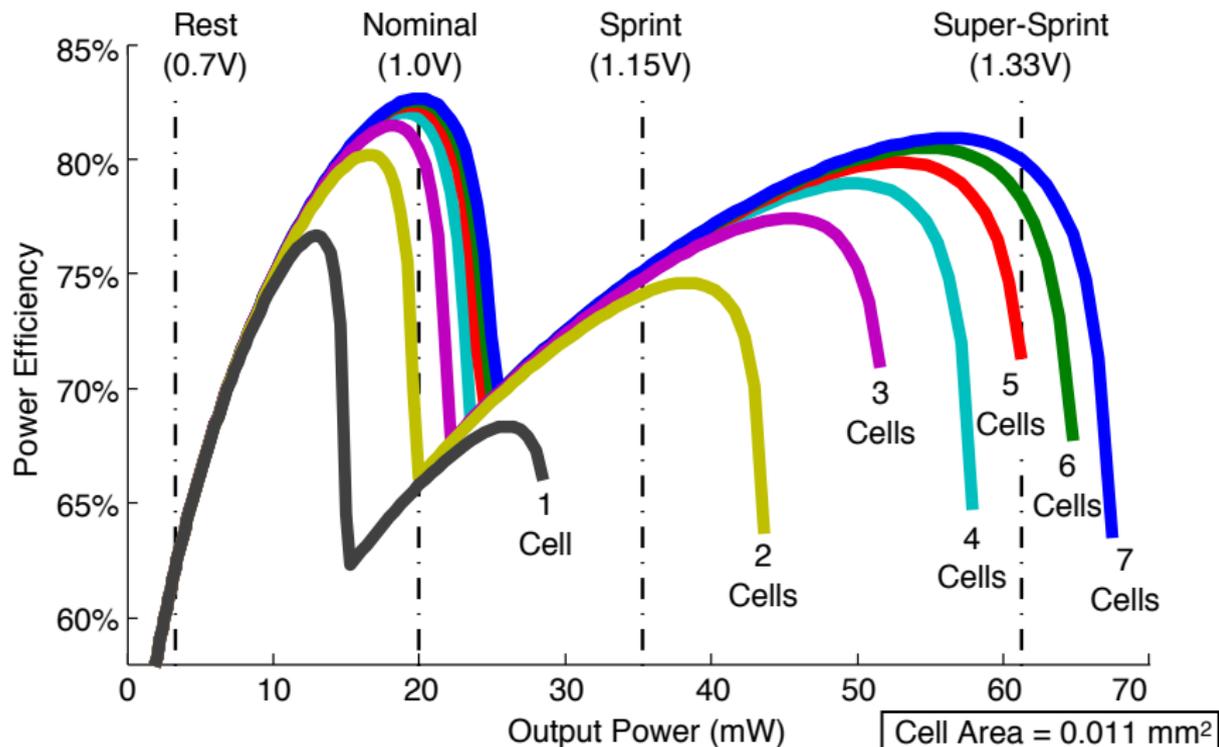
MAVR: Per-Core Regulator Sizing Study

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MAVR: Multiple Adjustable Voltage Regulators
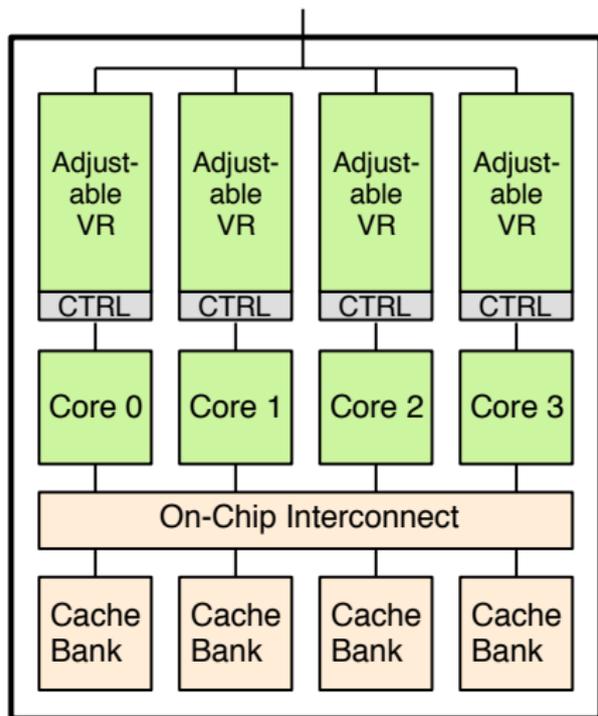
MAVR

MAVR: Multiple Adjustable Voltage Regulators
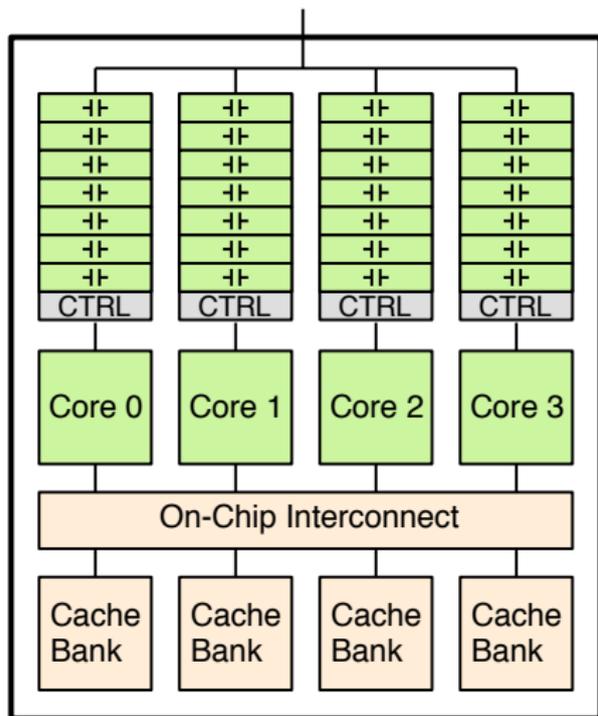
MAVR

MAVR: Multiple Adjustable Voltage Regulators
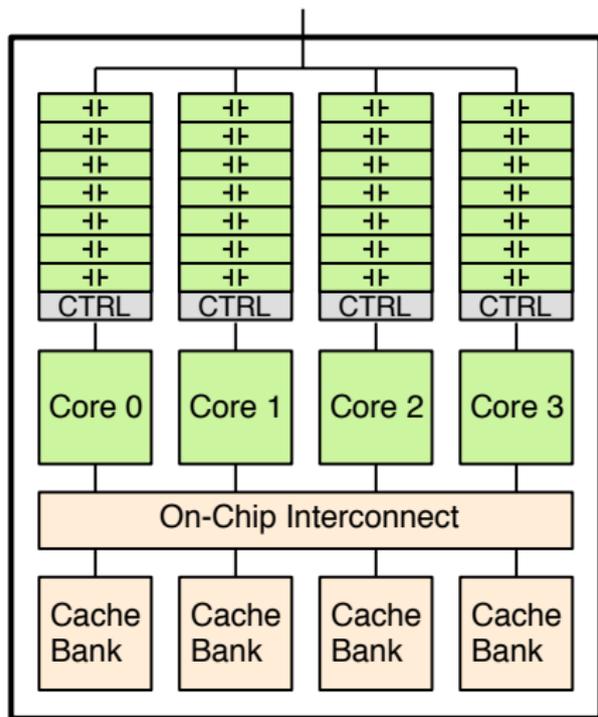
MAVR

Key Observation

MAVR requires enough area for each regulator to independently support all power modes

Power limits mean FG-SYNC+ is designed such that only 1 or 2 cores are ever super-sprinting at once

RPDN: Reconfigurable Power Distribution Networks

MAVR

RPDN

RPDN: Reconfigurable Power Distribution Networks
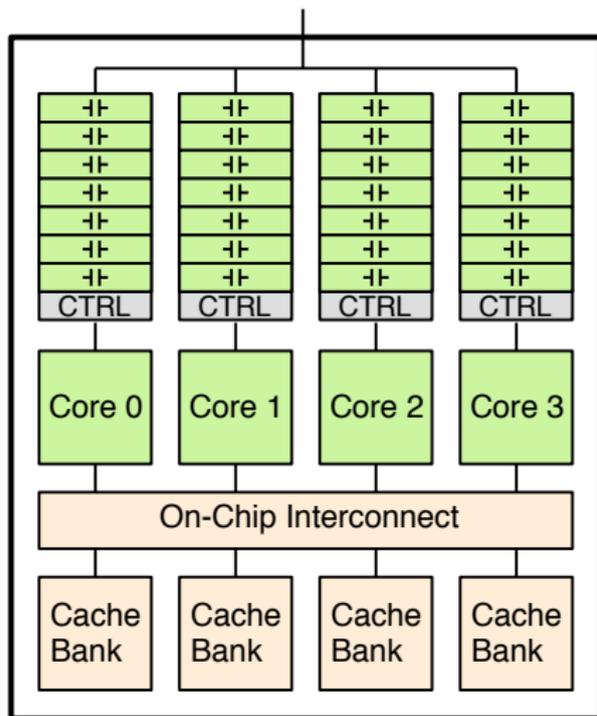
MAVR
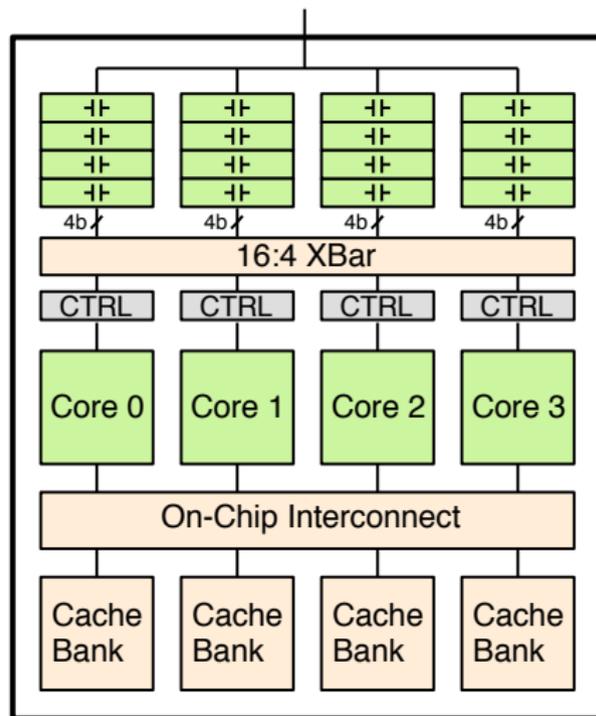
RPDN

RPDN: Reconfigurable Power Distribution Networks

40% Area Savings
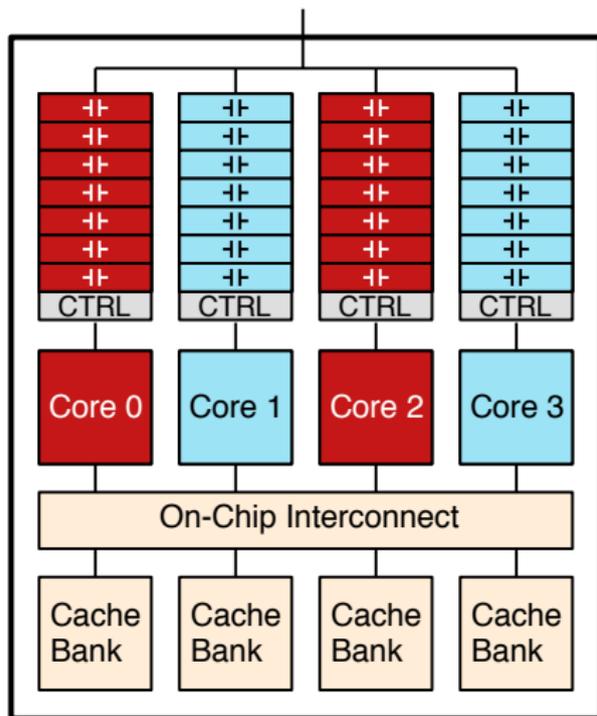
MAVR

RPDN

SPICE-Level Transient Response + Leakage Benefits

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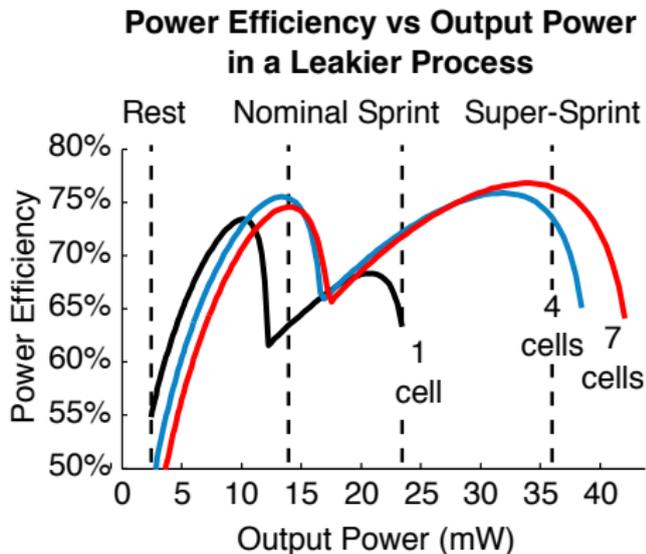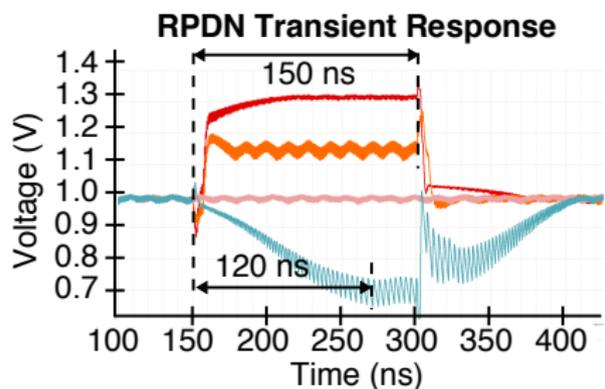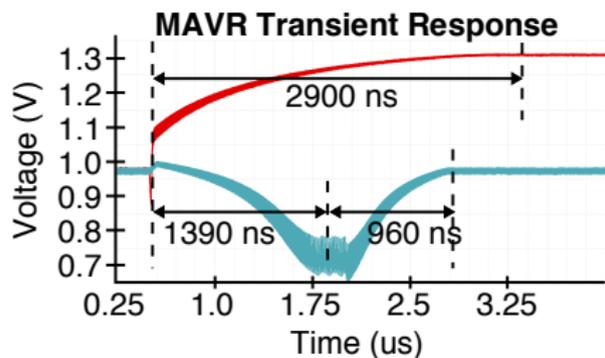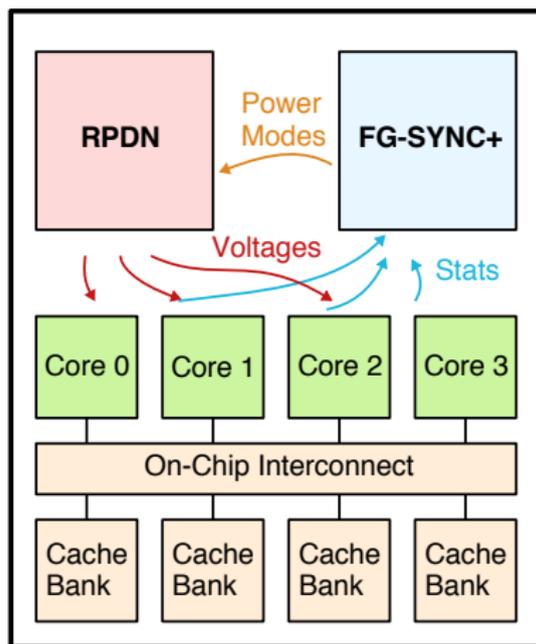
MAVR Transient Response

RPDN Transient Response

Power Efficiency vs Output Power in a Leakier Process
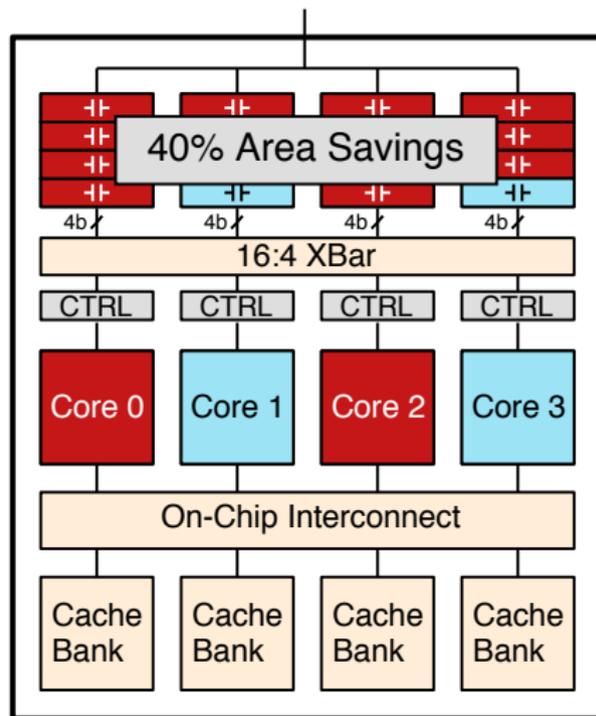
Talk Outline

FGVS Architecture: FG-SYNC+

Use lightweight software hints and lookup tables derived offline to enable fast multi-level voltage configuration

FGVS Circuits: RPDN

Enable sprinting cores to dynamically borrow energy storage from resting cores

Methodology and Evaluation

Architecture and Circuits Co-Design Approach

Methodology

C++ Multithreaded
App Using Hints

↓

Cross
Compiler

↓

RISC Binary

↓

RISC
ISA Sim

Cycle-Level Multicore
with DVFS Controller

↓

Cycle-Level
Simulator
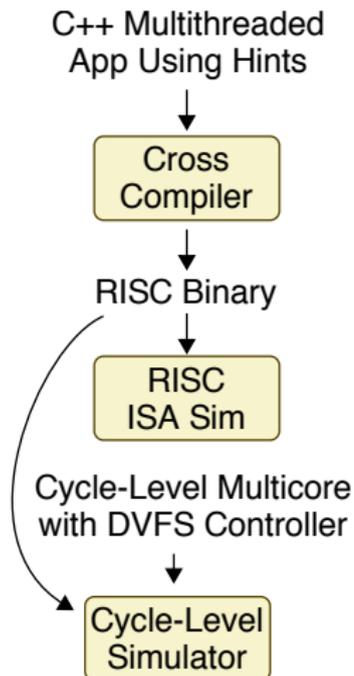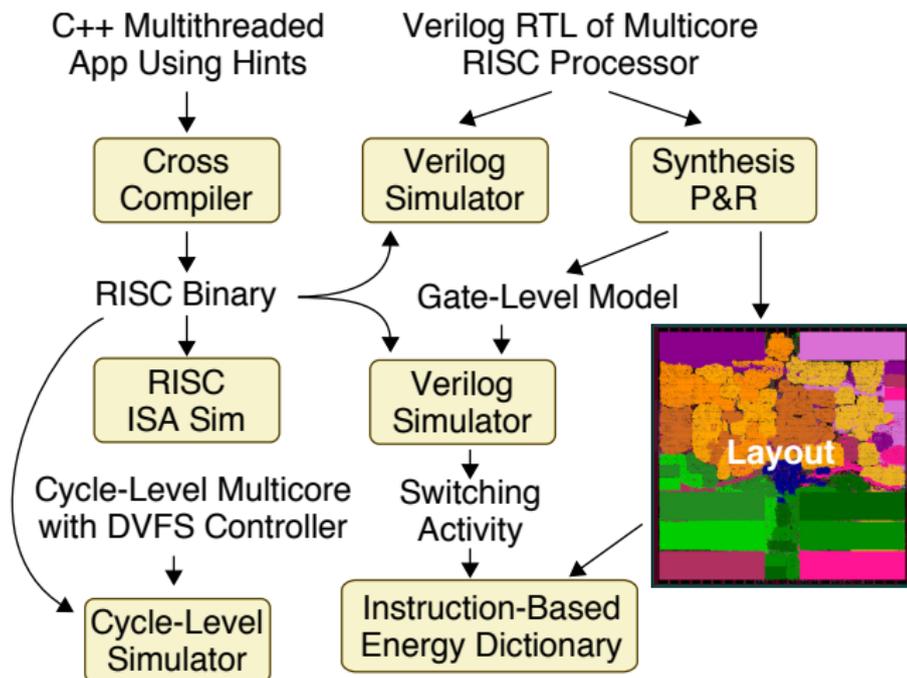
Methodology
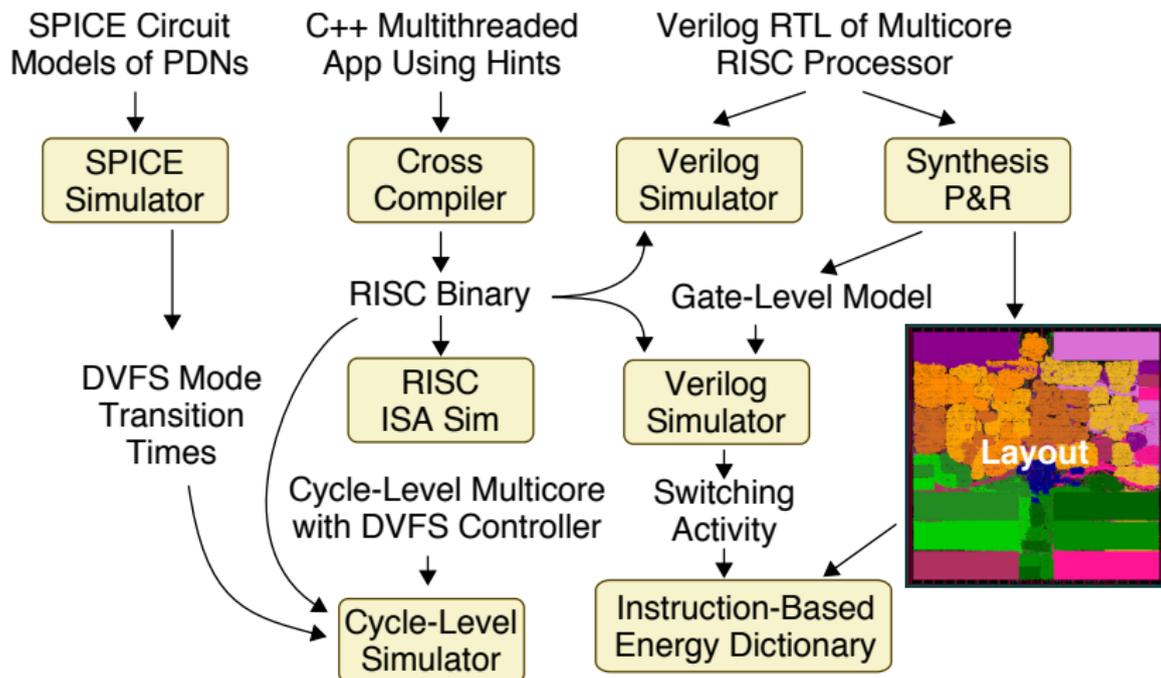
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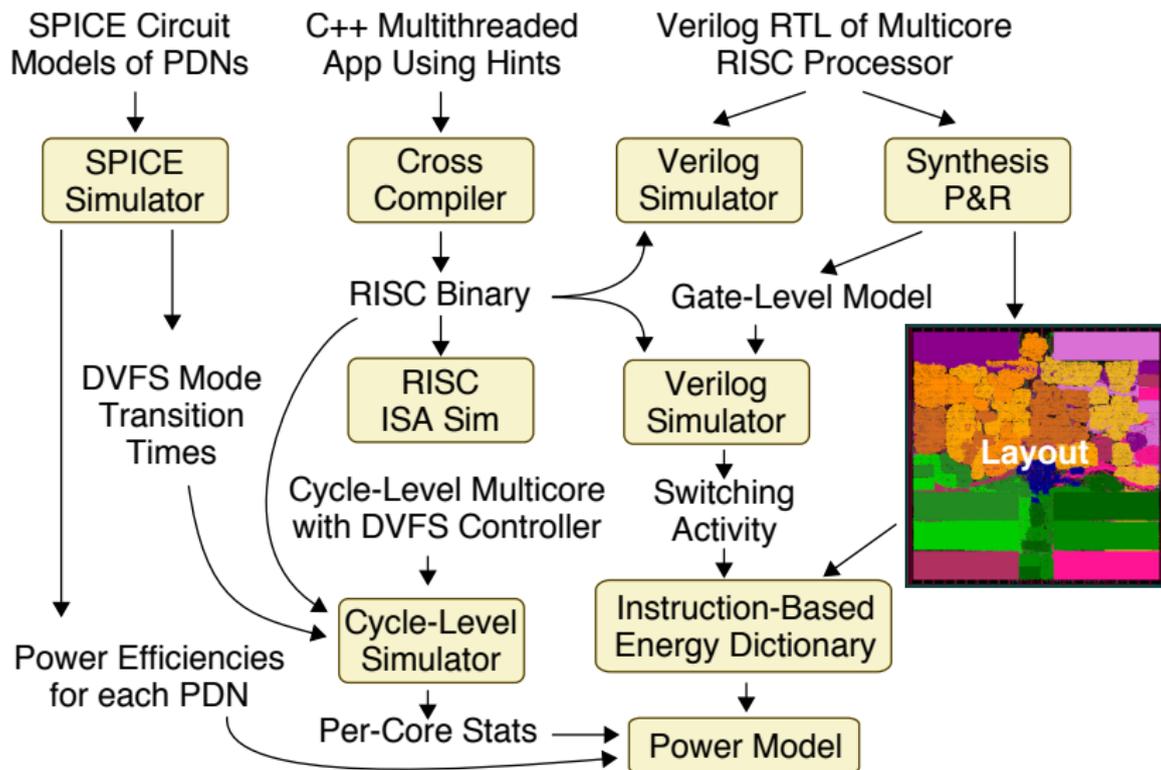
Methodology

Methodology

Evaluation

Benchmarks

▶ bfs

▶ bilateral

▶ dither

▶ kmeans

▶ mriq

▶ pbbs-dr

▶ pbbs-knn

▶ pbbs-mm

▶ rsort

▶ splash2-fft

▶ splash2-lu

▶ strsearch

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Evaluation

■ No FGVS   ● MAVR   ◆ RPDN

2X Performance Boost with 40% Area Savings over MAVR

Benchmarks

▶ bfs

▶ bilateral

▶ dither

▶ kmeans

▶ mriq

▶ pbbs-dr

▶ pbbs-knn

▶ pbbs-mm

▶ rsort

▶ splash2-fft

▶ splash2-lu

▶ strsearch

▶ viterbi

Evaluation

2X Performance Boost with 40% Area Savings over MAVR
10-50% Performance and 10-70% Energy Eff. over no FGVS

Benchmarks

▶ bfs

▶ bilateral

▶ dither

▶ kmeans

▶ mriq

▶ pbbs-dr

▶ pbbs-knn

▶ pbbs-mm

▶ rsort

▶ splash2-fft

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▶ strsearch

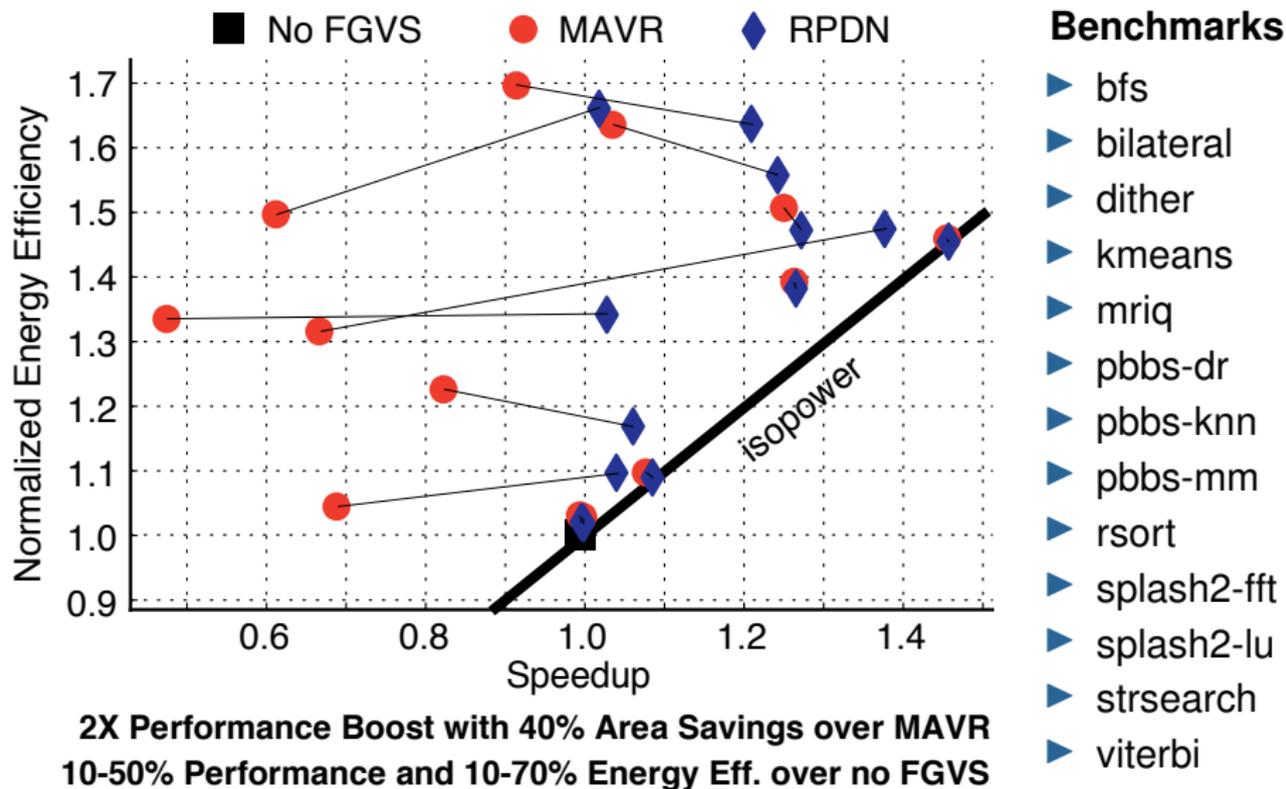▶ viterbi

Take-Away Points

▶ **Architecture and Mixed-Signal Circuit Co-Design** can maximize the system-level benefit of the emerging trend towards integrated voltage regulation.

▶ **Lightweight hints** can provide an elegant solution to informing hardware of fine-grain activity imbalance.

▶ **Reconfigurable Power Distribution Networks** can enable realistic FGVS by significantly reducing regulator area overhead and improving voltage-settling response times by an order of magnitude.