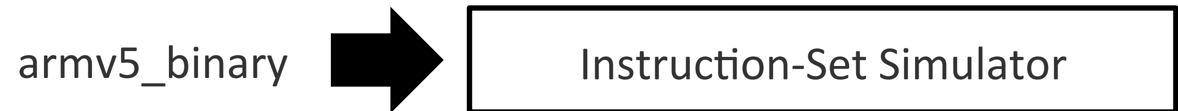
Pydgin: Generating Fast Instruction Set Simulators from Simple Architecture Descriptions with Meta-Tracing JIT Compilers

Derek Lockhart, Berkin Ilbeyi, and Christopher Batten

Cornell University
Computer Systems Laboratory

Motivation

Instruction set simulators perform **functional** simulation of a target architecture.



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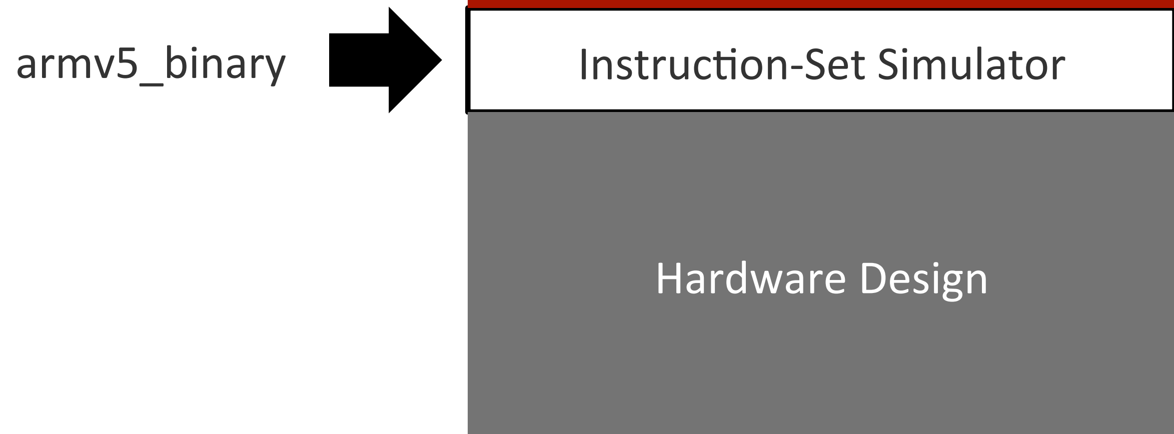

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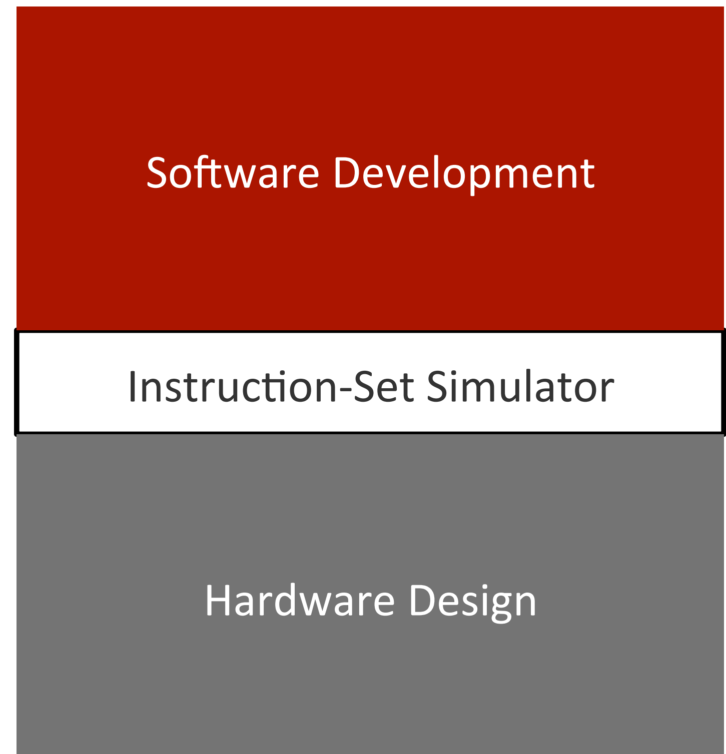
Instruction-Set Simulator Goals:

- Accuracy
- Observability
- Performance



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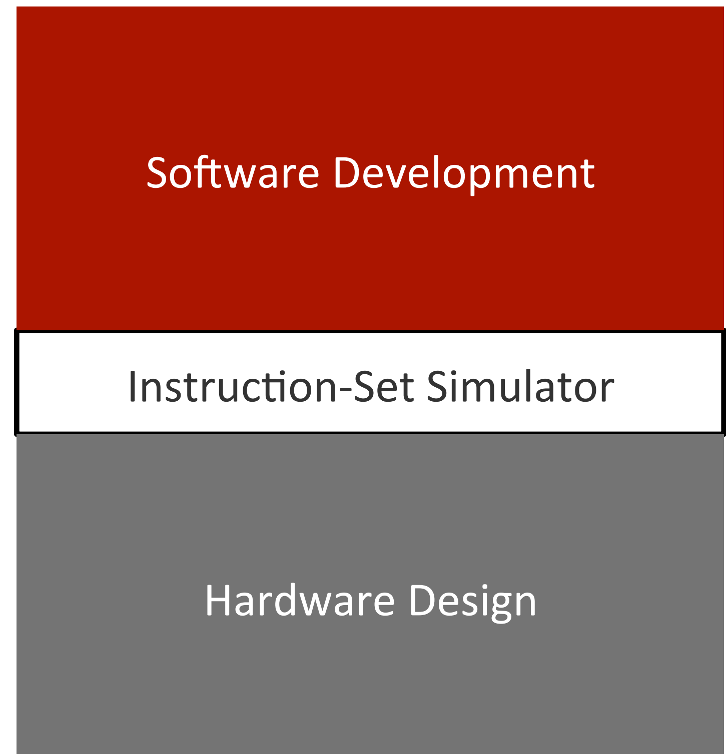

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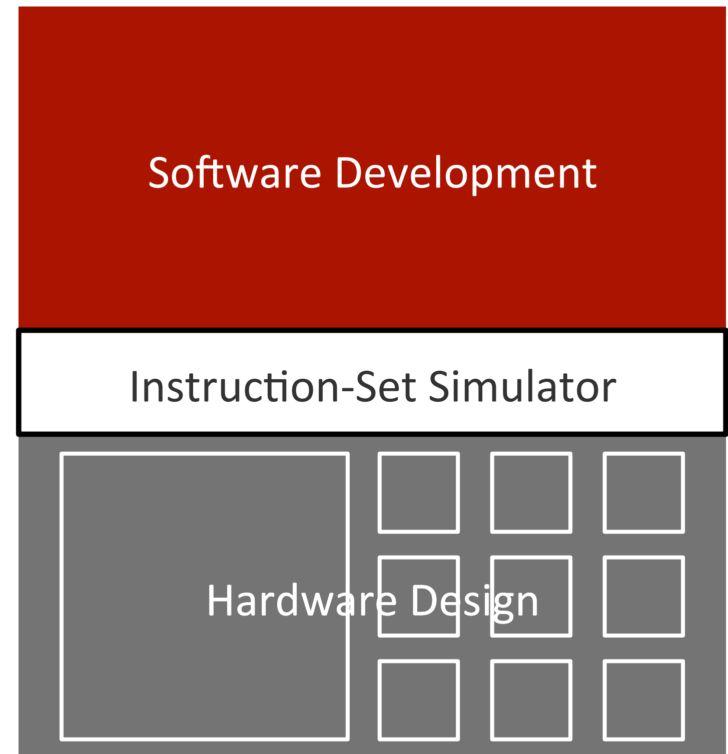

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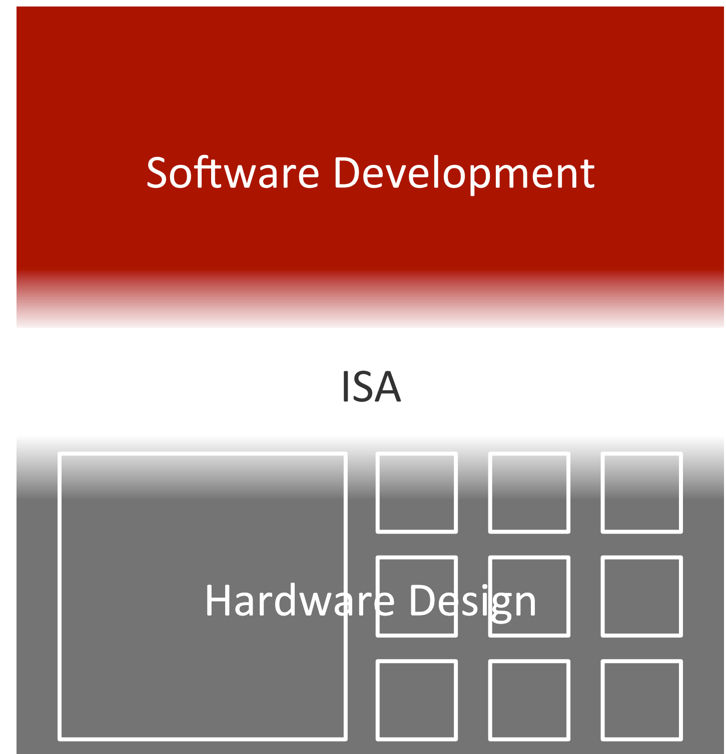

Productivity Performance

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Architectural Description Language

Instruction Set Interpreter in C with DBT

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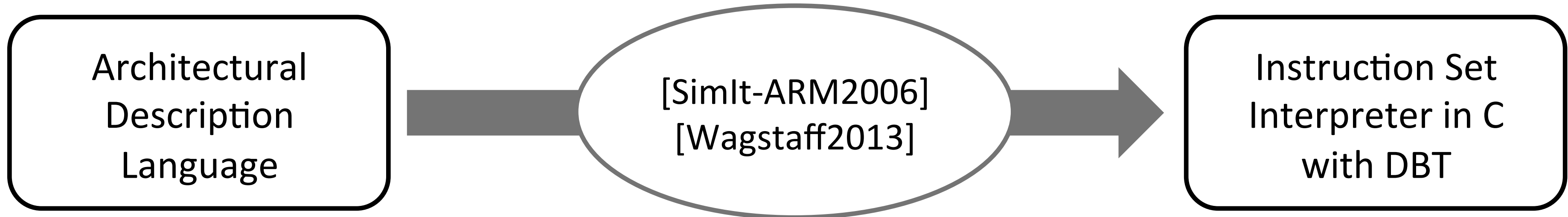

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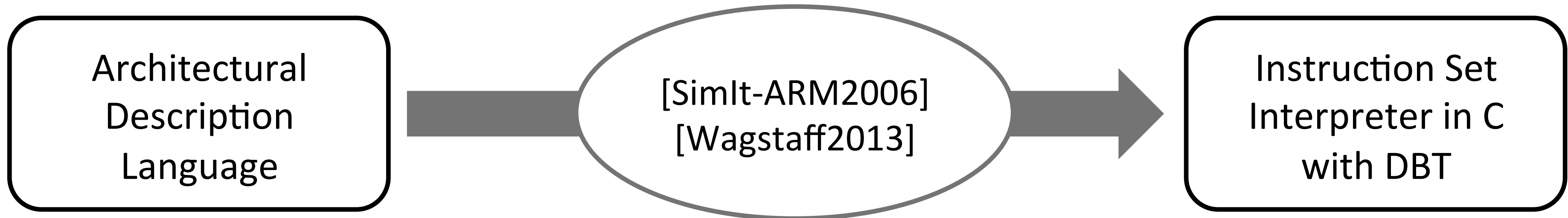

[Simit-ARM2006]

+ Page-based JIT
- Ad-hoc ADL with custom parser
- Unmaintained

[Wagstaff2013]

+ Region-based JIT
+ Industry-supported ADL (ArchC)
- C++-based ADL is verbose
- Not Public

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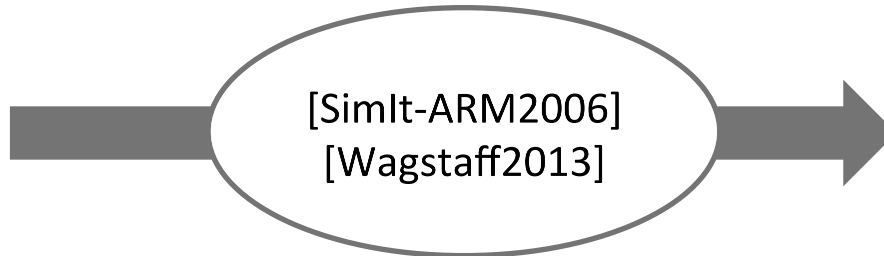

Instruction Set Interpreter in C with DBT

Dynamic Language Interpreter in C with JIT Compiler

Productivity Performance

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Instruction Set Interpreter in C with DBT

Key Insight:

Similar productivity-performance challenges for building high-performance interpreters of dynamic languages.
(e.g. JavaScript, Python)

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Dynamic Language Interpreter in C with JIT Compiler

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Architectural Description Language → [SimIt-ARM2006] [Wagstaff2013] → Instruction Set Interpreter in C with DBT

Dynamic-Language Interpreter in RPython → RPython Translation Toolchain → Dynamic Language Interpreter in C with JIT Compiler

Productivity

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pypy

Dynamic-Language Interpreter in RPython → RPython Translation Toolchain → Dynamic Language Interpreter in C with JIT Compiler

Meta-Tracing JIT:
makes JIT generation generic across languages

Productivity

Performance

Architectural Description Language

Instruction Set Interpreter in C with DBT

RPython Translation Toolchain

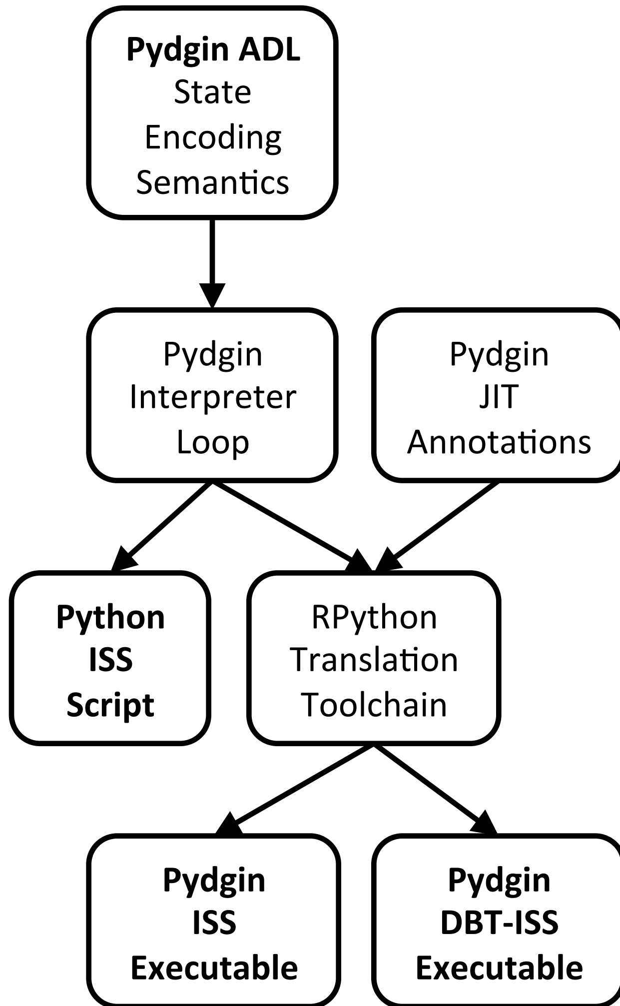
Productivity Performance

Architectural Description Language

Instruction Set Interpreter in C with DBT

- Flexible, productive, pseudocode-like ADL syntax
- ADL embedded in a popular, general-purpose language
- Tracing-JIT generator applies across many different ISAs
- Leverages advancements from dynamic-language JIT research

Pydgin Framework



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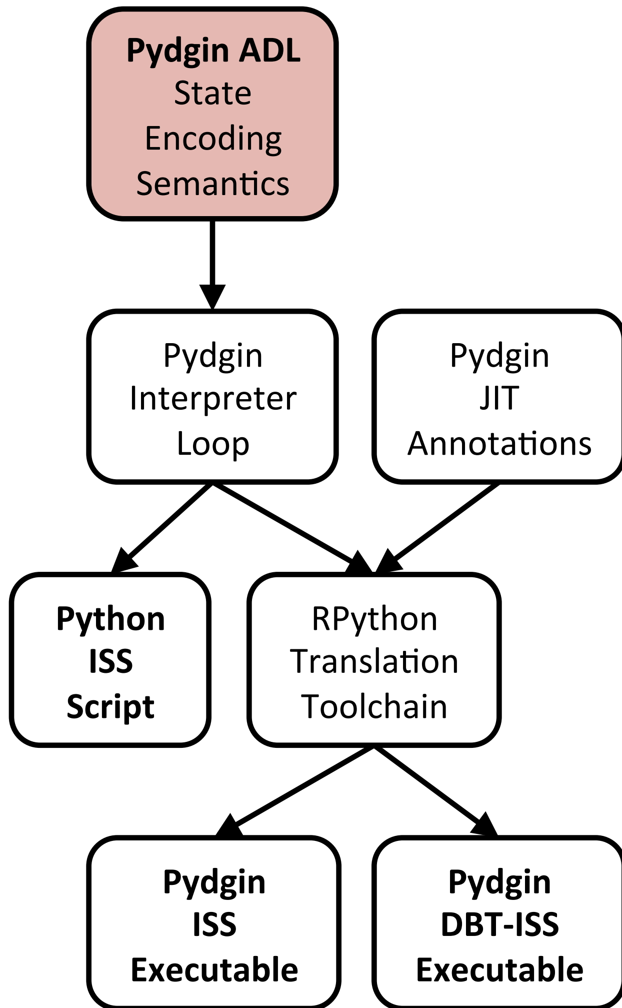
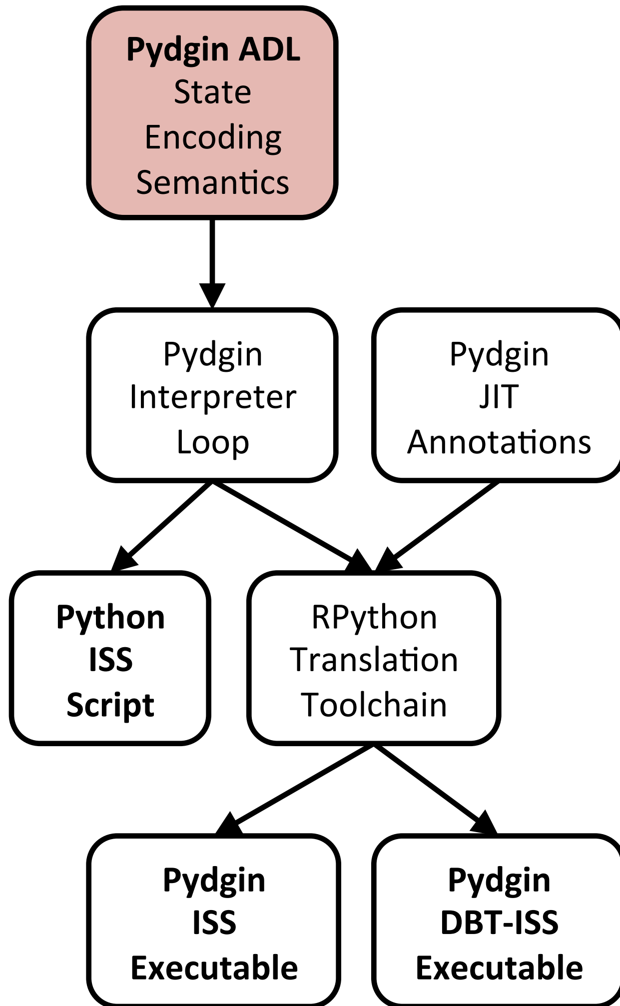


Pydgin ADL: ARMv5 Architectural State

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class State( object ):

  def __init__( self, memory, reset_addr=0x400 ):
    self.pc  = reset_addr
    self.rf  = ArmRegisterFile( self, num_regs=16 )
    self.mem = memory

    self.rf[ 15 ] = reset_addr

    # current program status register (CPSR)
    self.N    = 0b0      # Negative condition
    self.Z    = 0b0      # Zero condition
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  def fetch_pc( self ):
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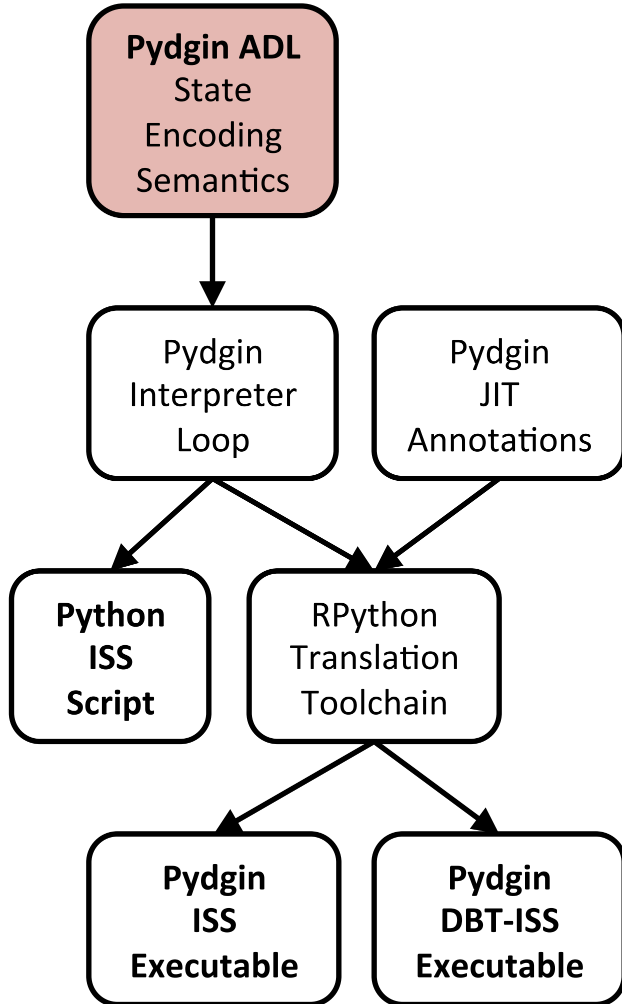


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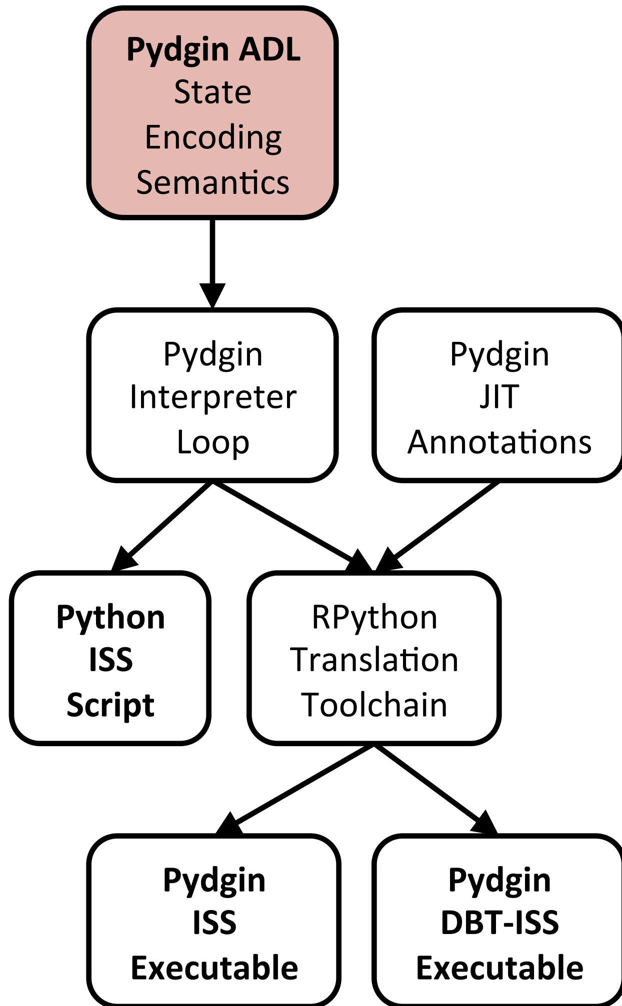


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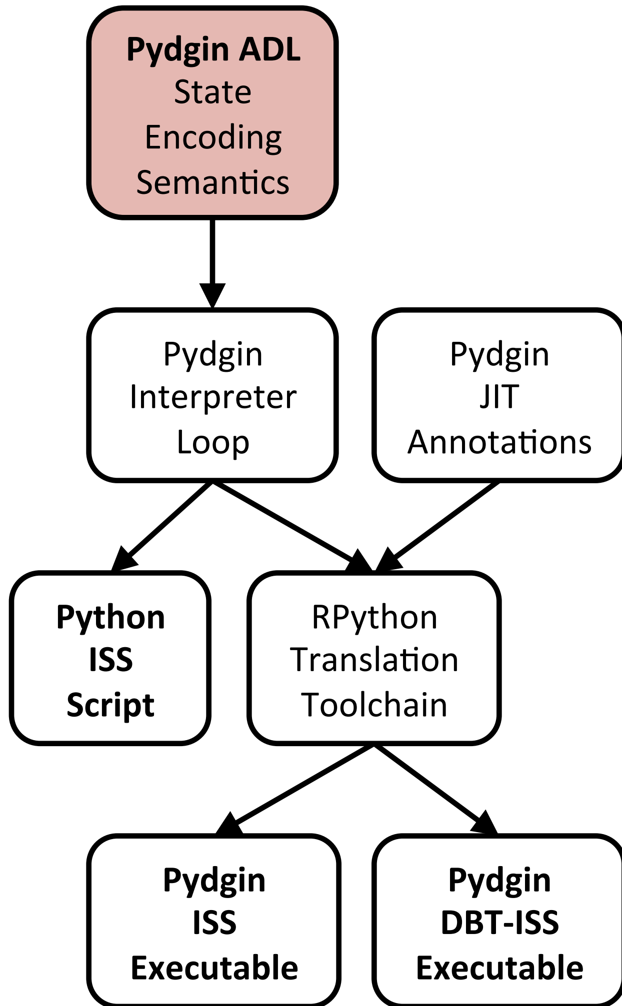


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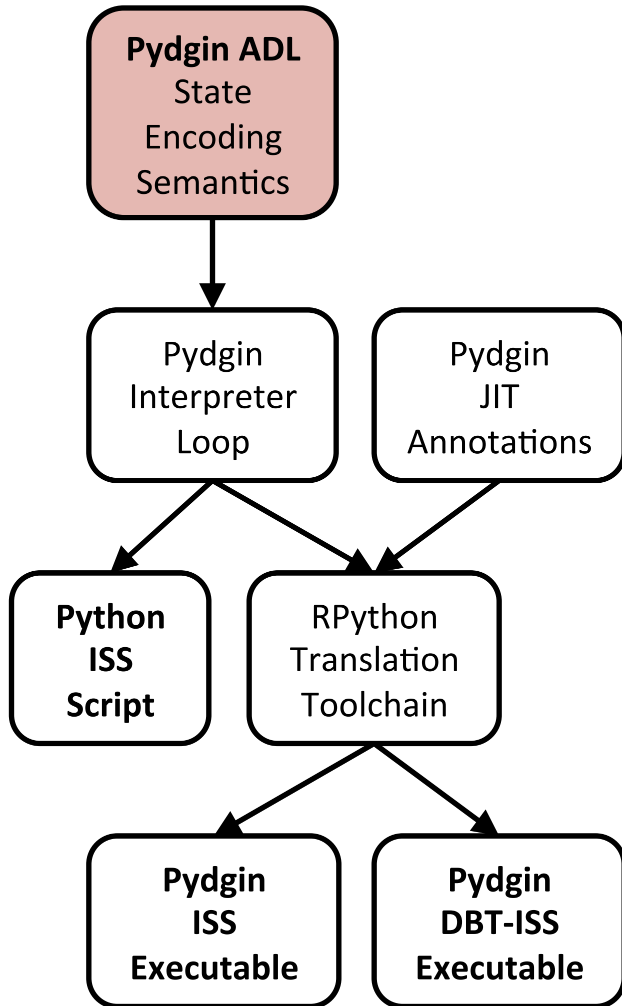


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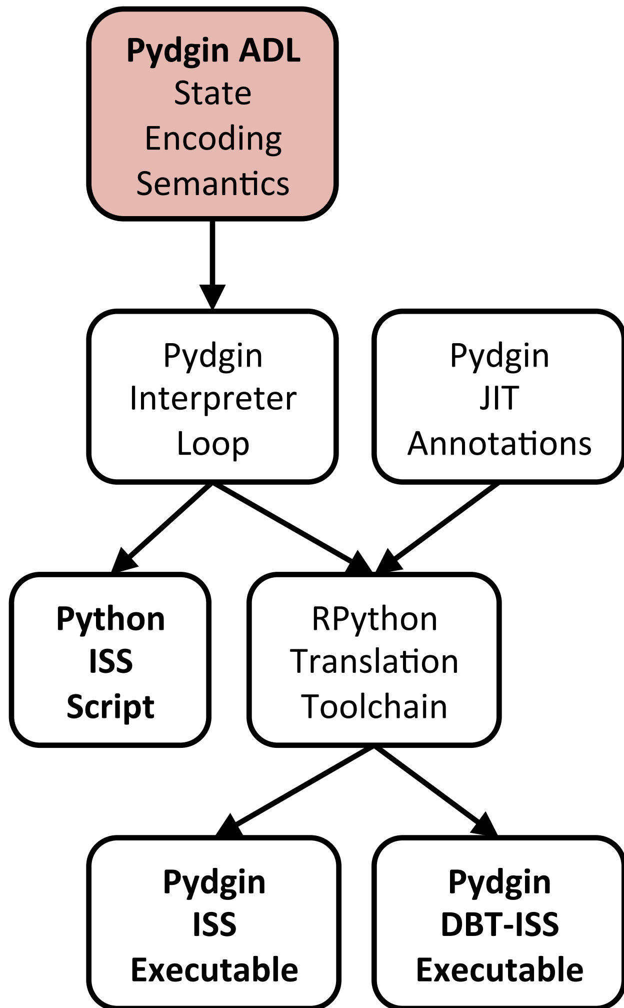


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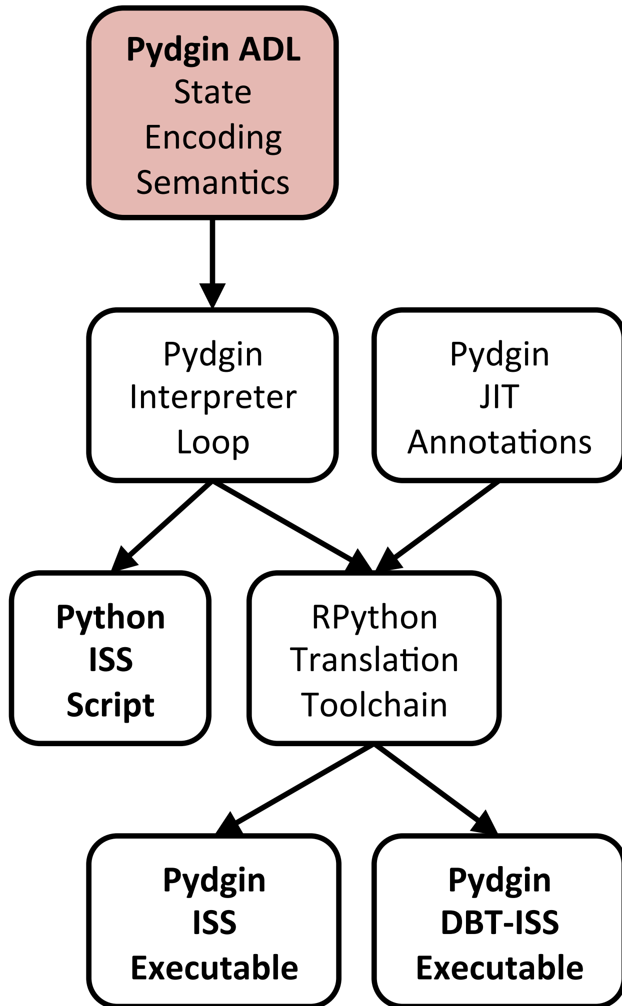


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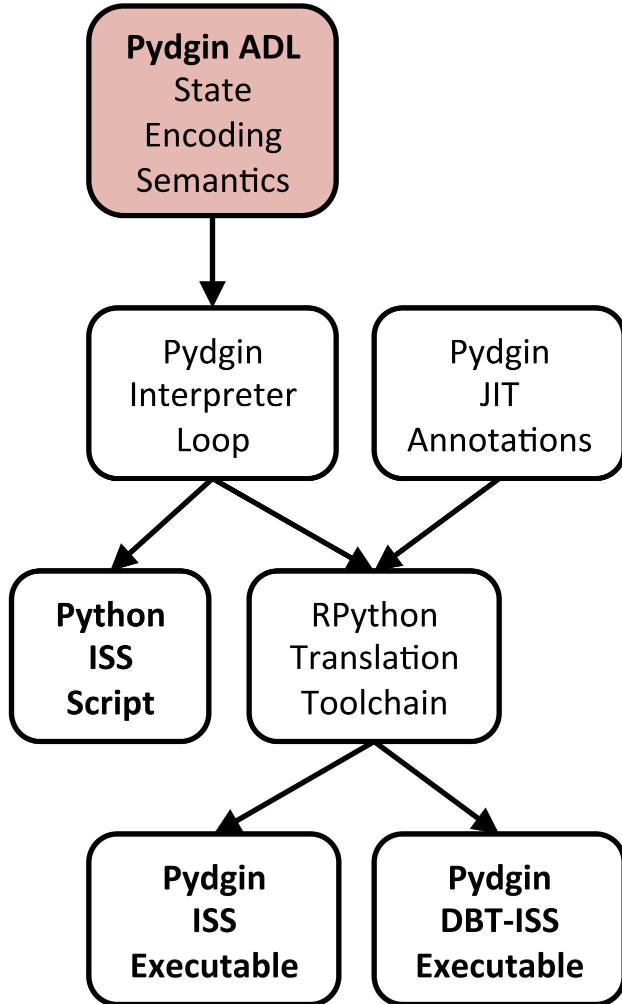


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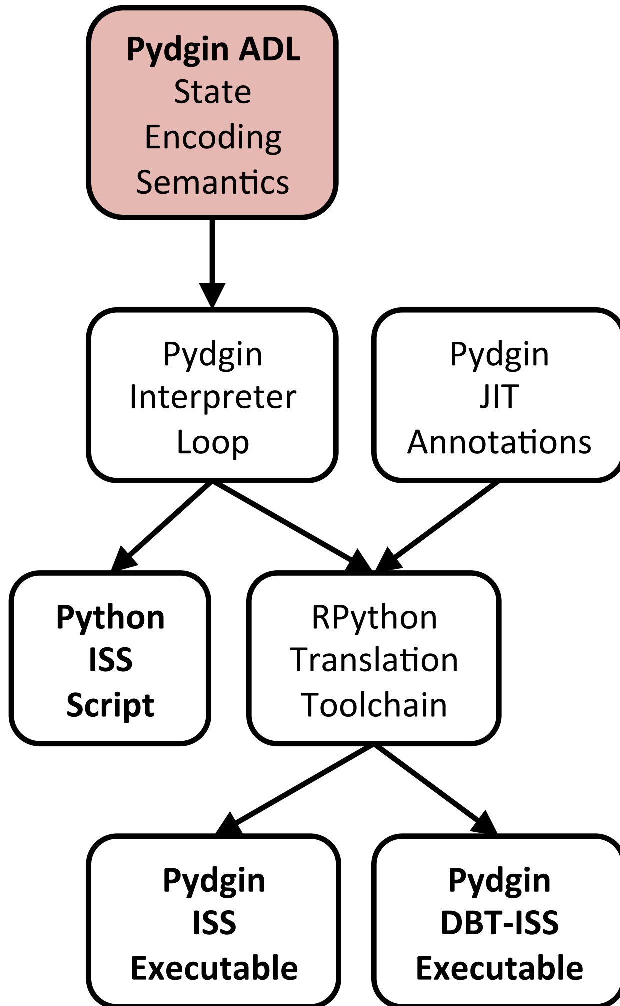


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    s.rf[ inst.rd() ] = trim_32(result)

    if inst.S():
      # ...
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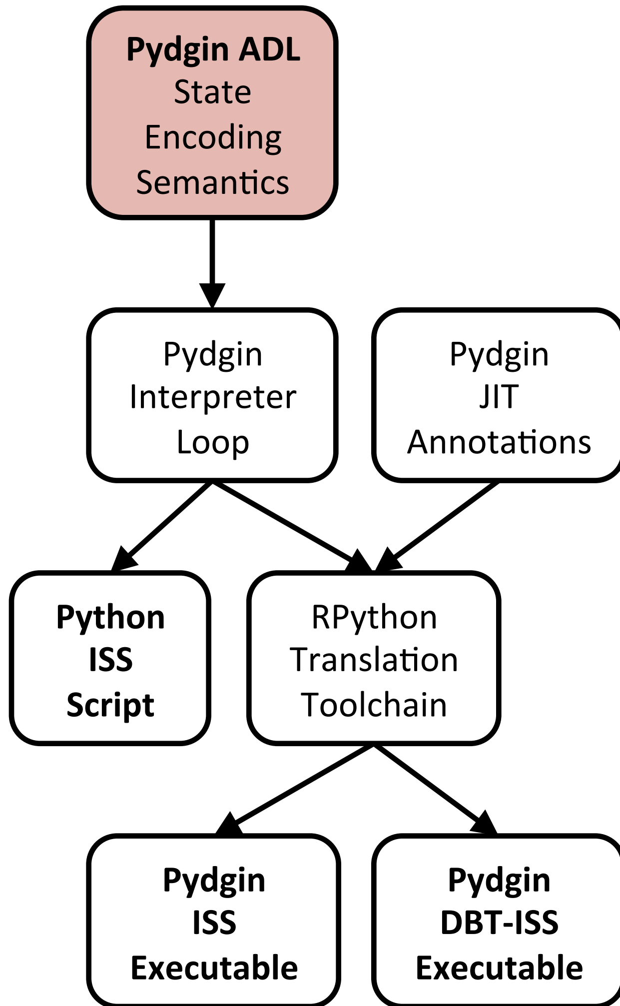


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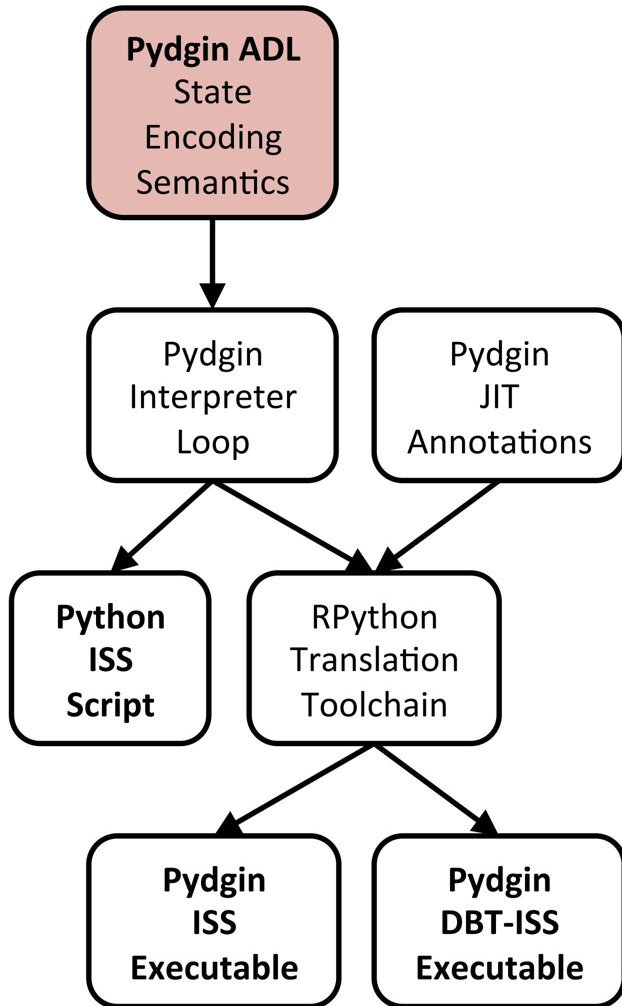


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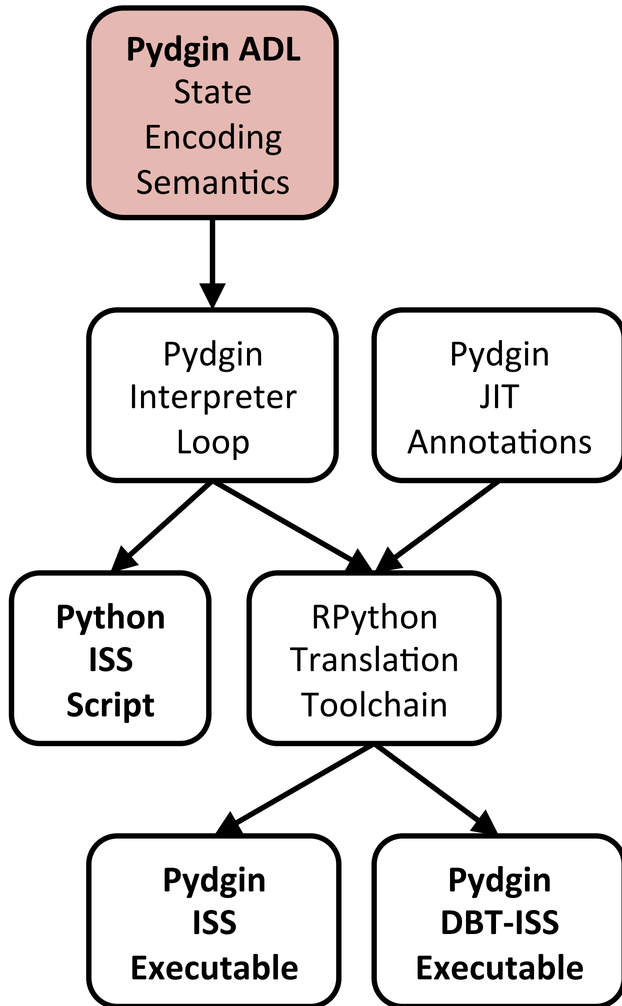


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Pydgin ADL
State

ARM ISA MANUAL SPEC

```
if ConditionPassed(cond) then

  Rd = Rn + shifter_operand

  if S == 1 and Rd == R15 then
    if CurrentModeHasSPSR() then
      CPSR = SPSR
    else UNPREDICTABLE

  else if S == 1 then
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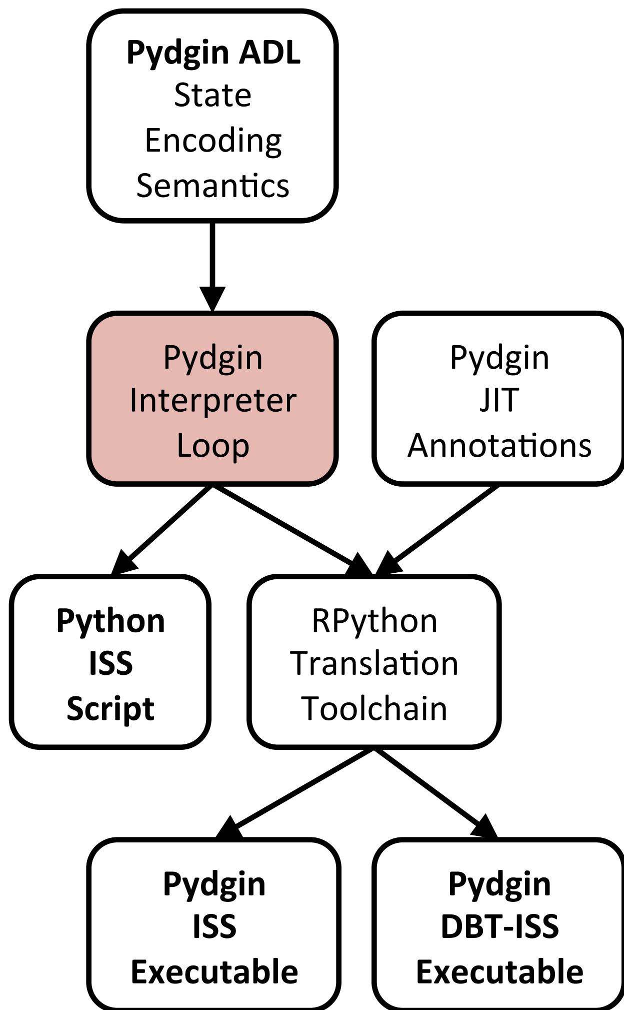

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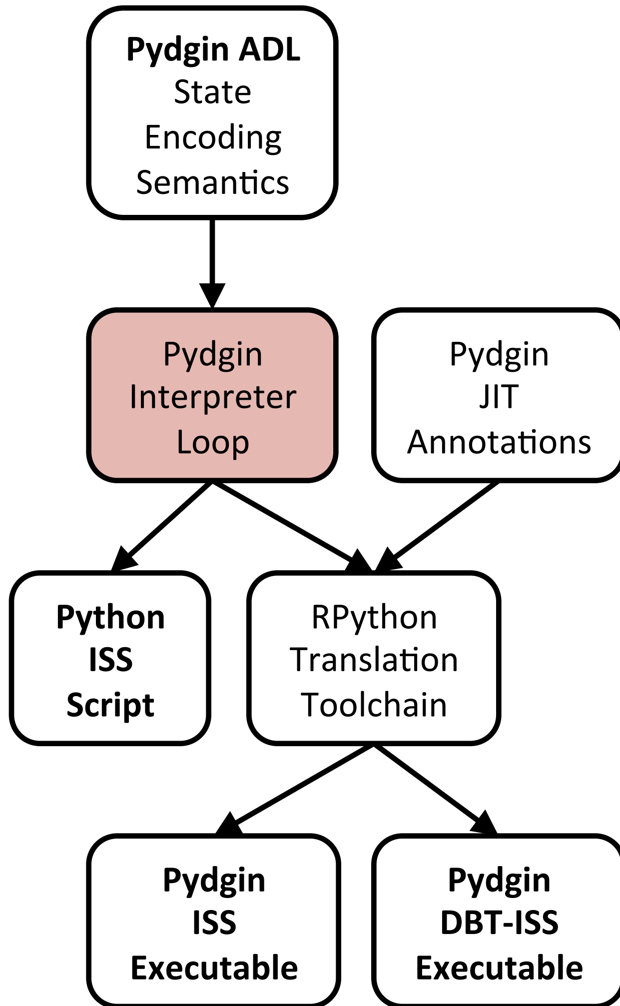


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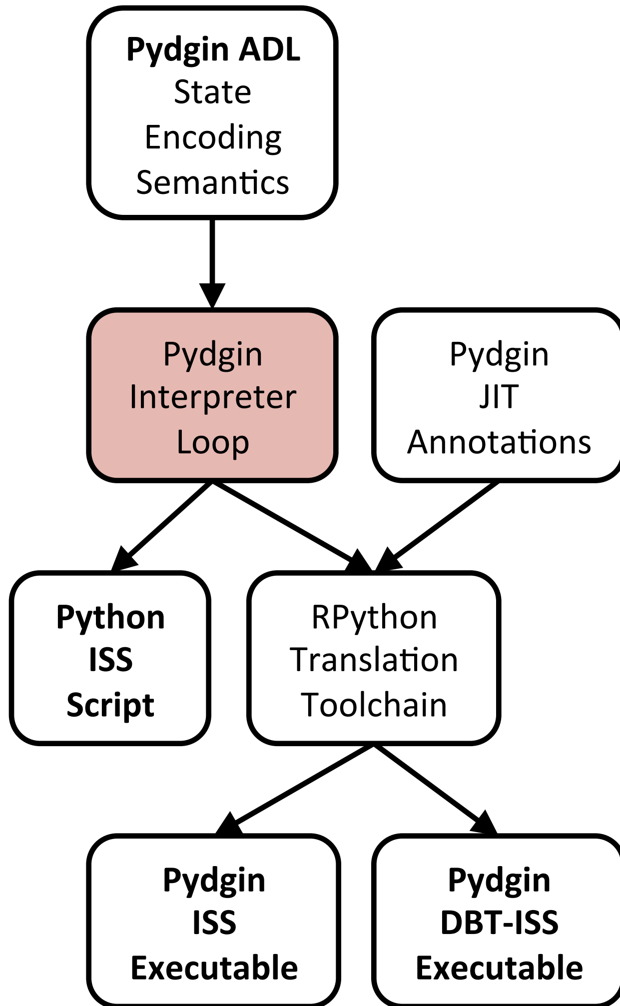


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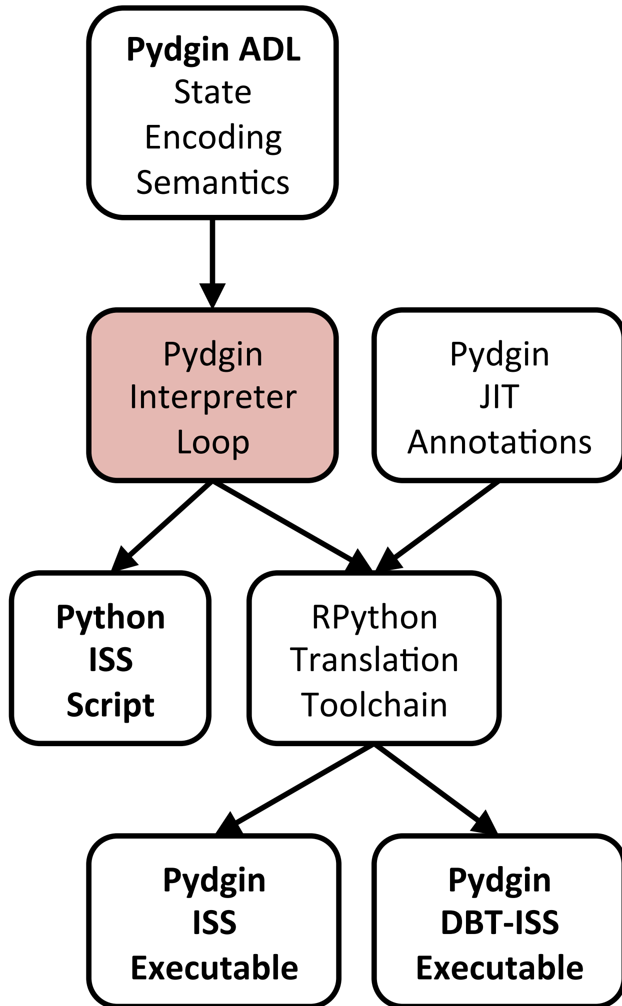


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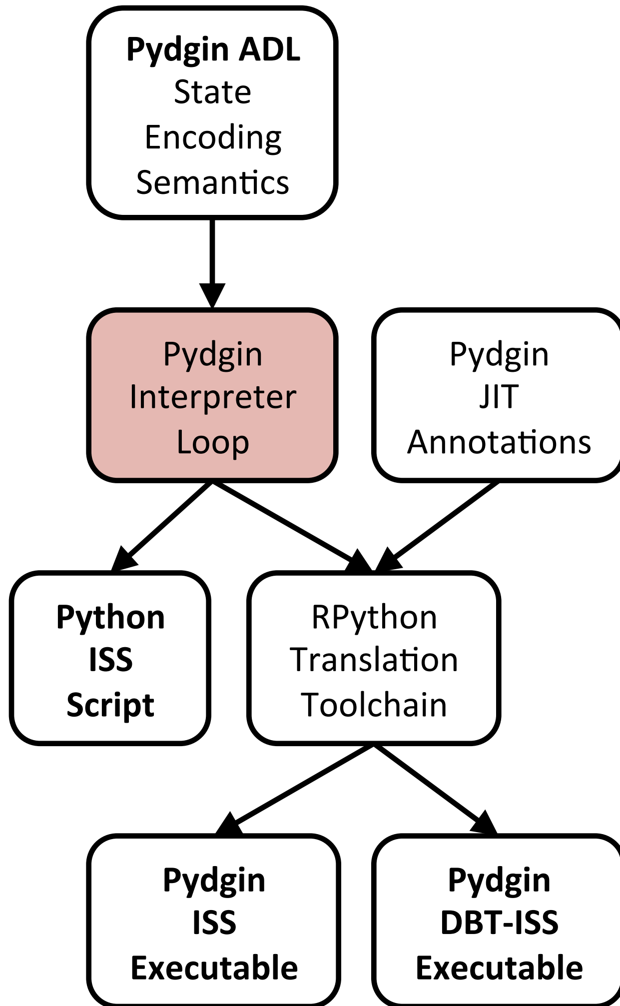


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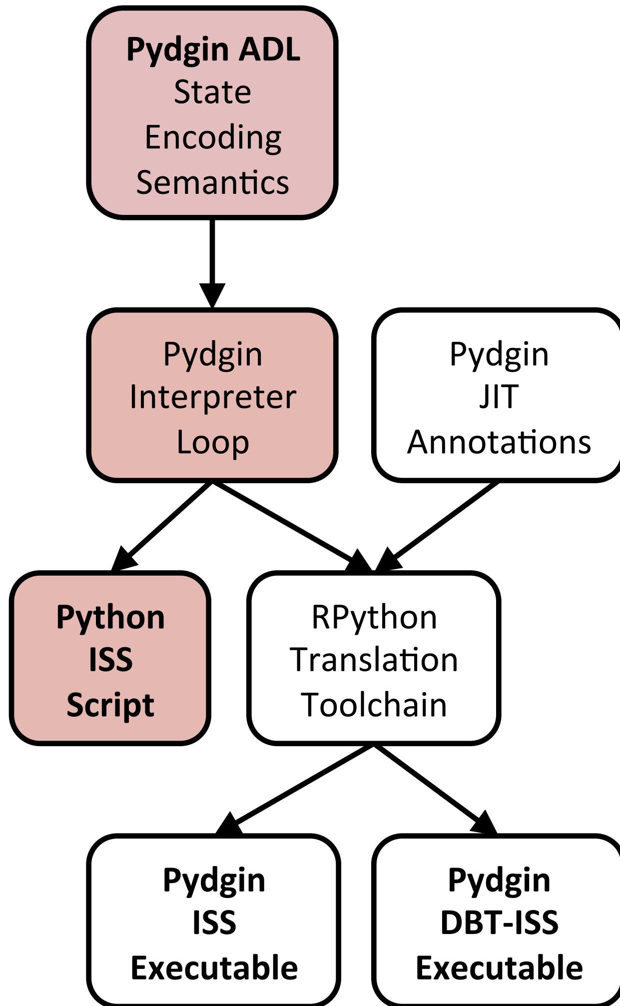


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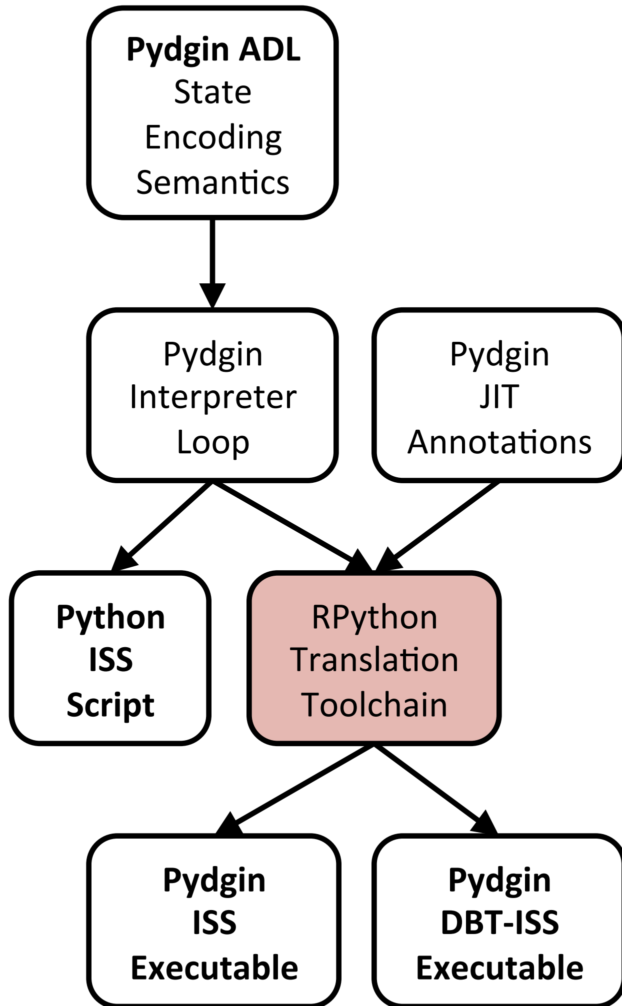
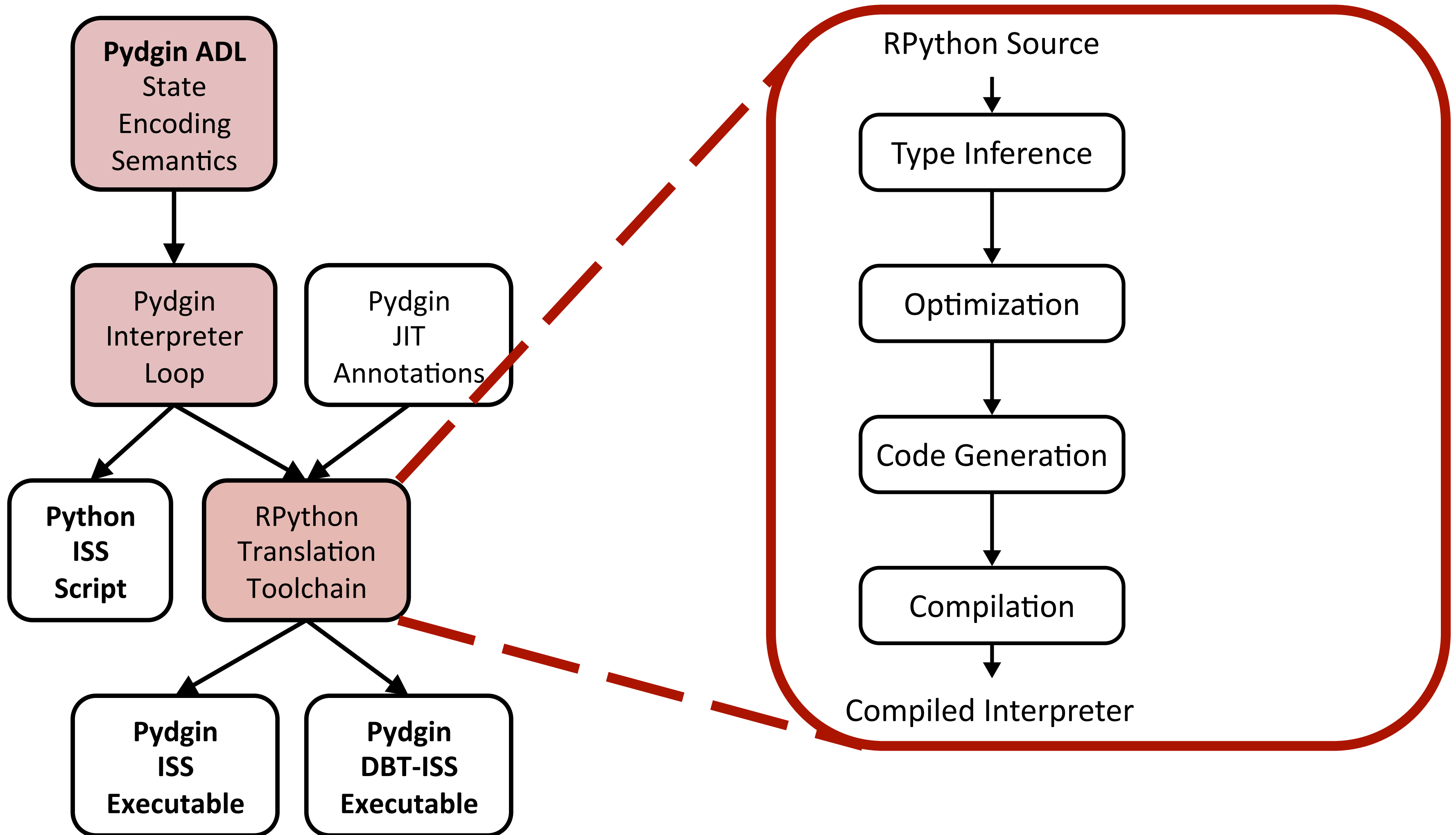
```
> python iss.py arm_binary
```

The RPython Translation Toolchain



The RPython Translation Toolchain



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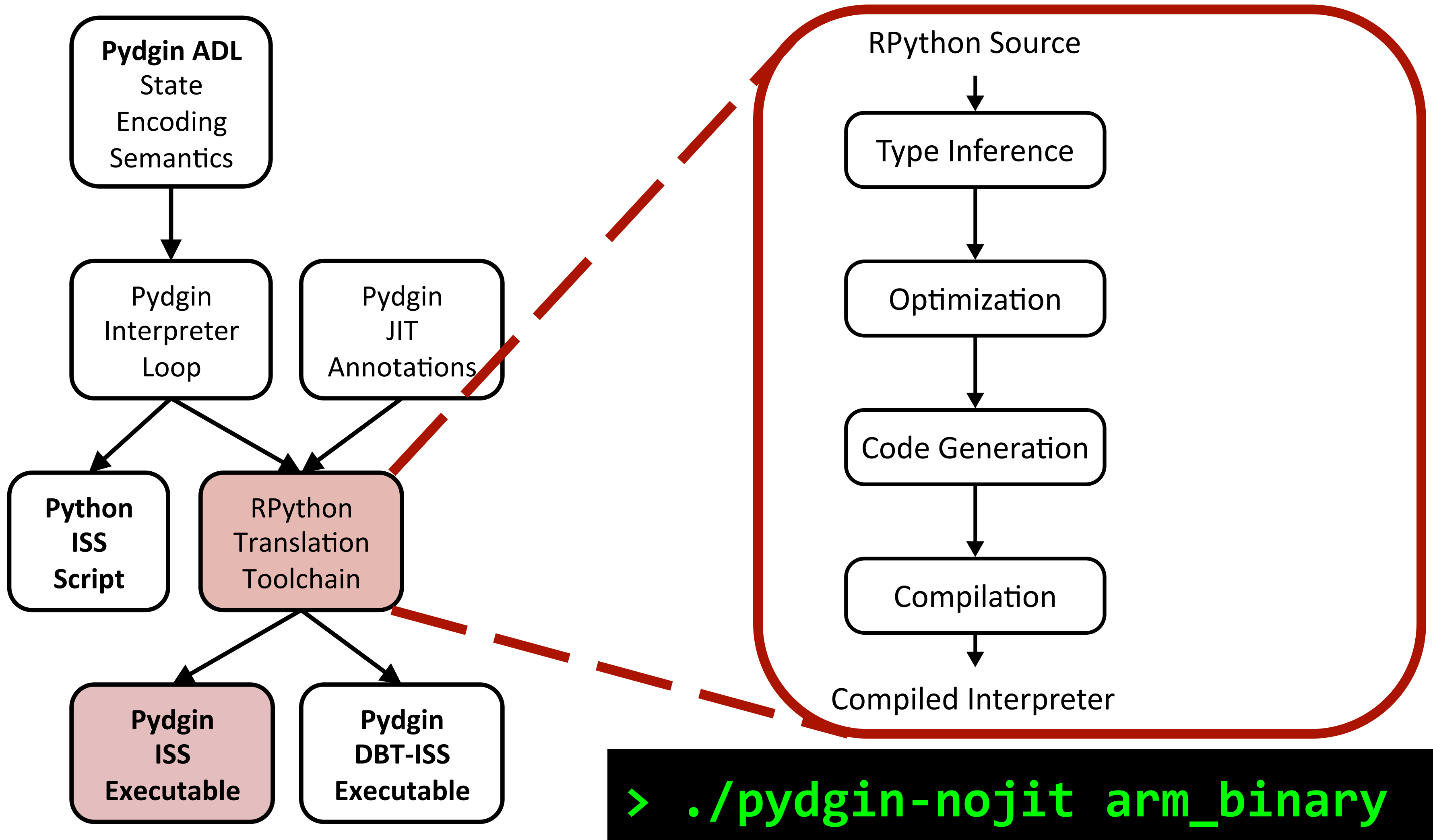
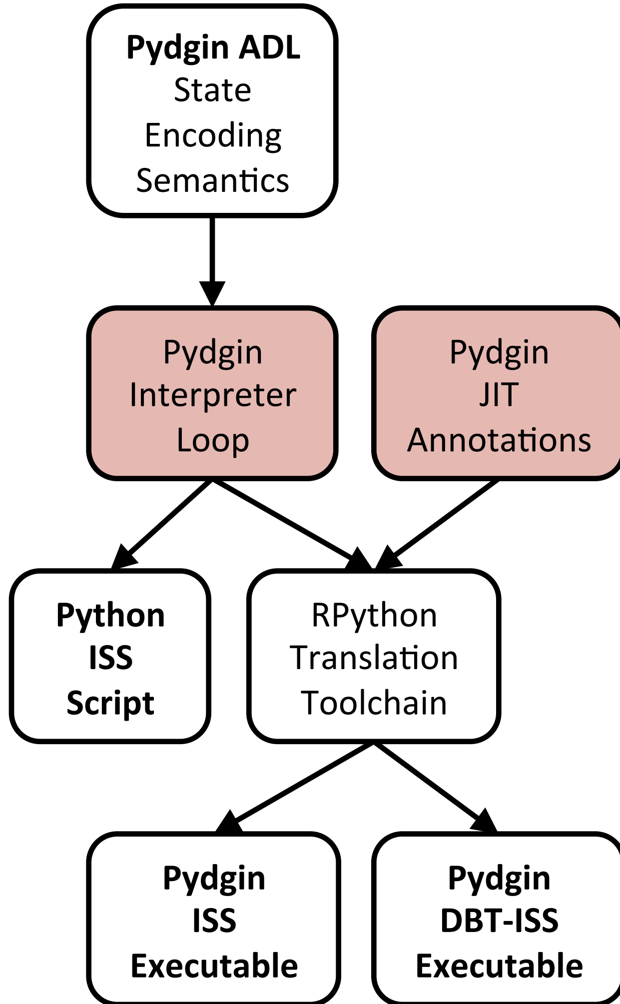


RPython ISS with JIT Annotations



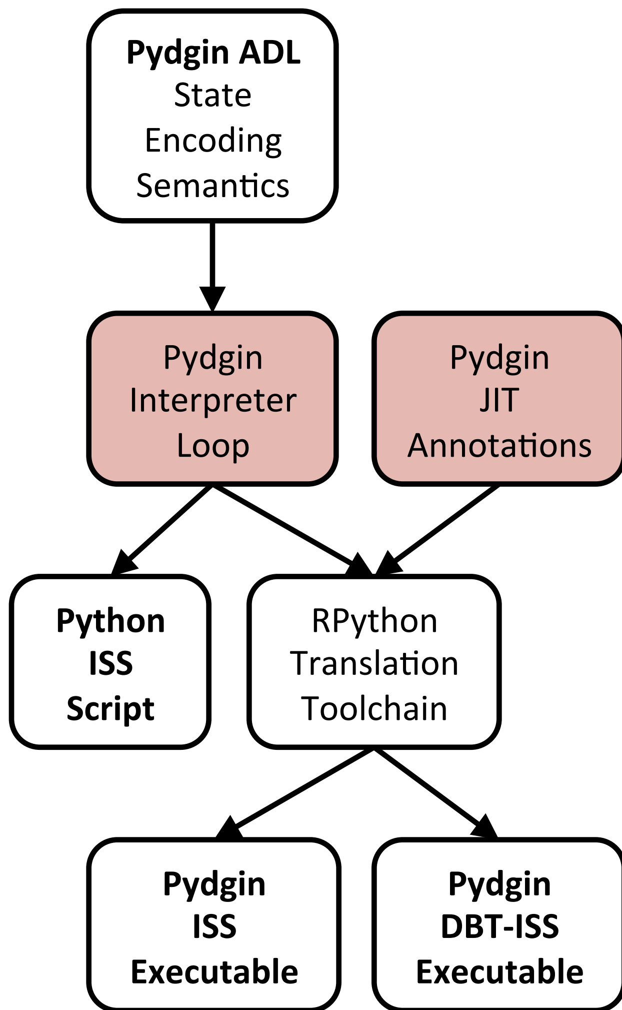

```
def instruction_set_interpreter( memory ):
  state = State( memory )

  while True:


    pc      = state.fetch_pc()

    inst    = memory[ pc ]       # fetch
    execute = decode( inst )     # decode
    execute( state, inst )       # execute
```

RPython ISS with JIT Annotations




```
jd = JitDriver( greens = ['pc'],
                reds   = ['state'] )

def instruction_set_interpreter( memory ):
  state = State( memory )

  while True:
    jd.jit_merge_point( s.fetch_pc(), state )

    pc      = state.fetch_pc()

    inst    = memory[ pc ]       # fetch
    execute = decode( inst )     # decode
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    if state.fetch_pc() < pc:
      jd.can_enter_jit( s.fetch_pc(), state )
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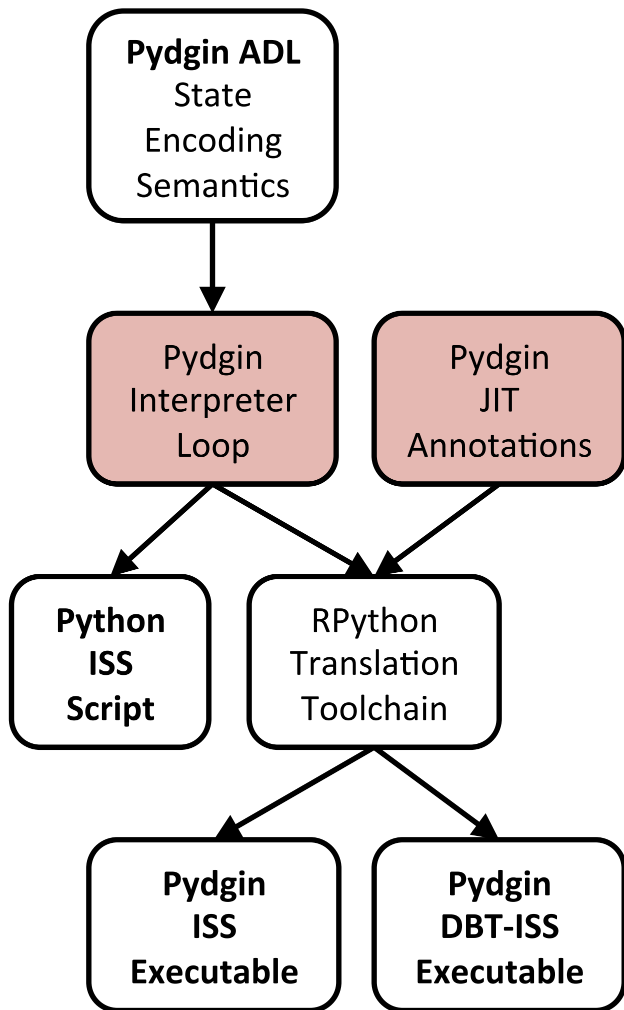


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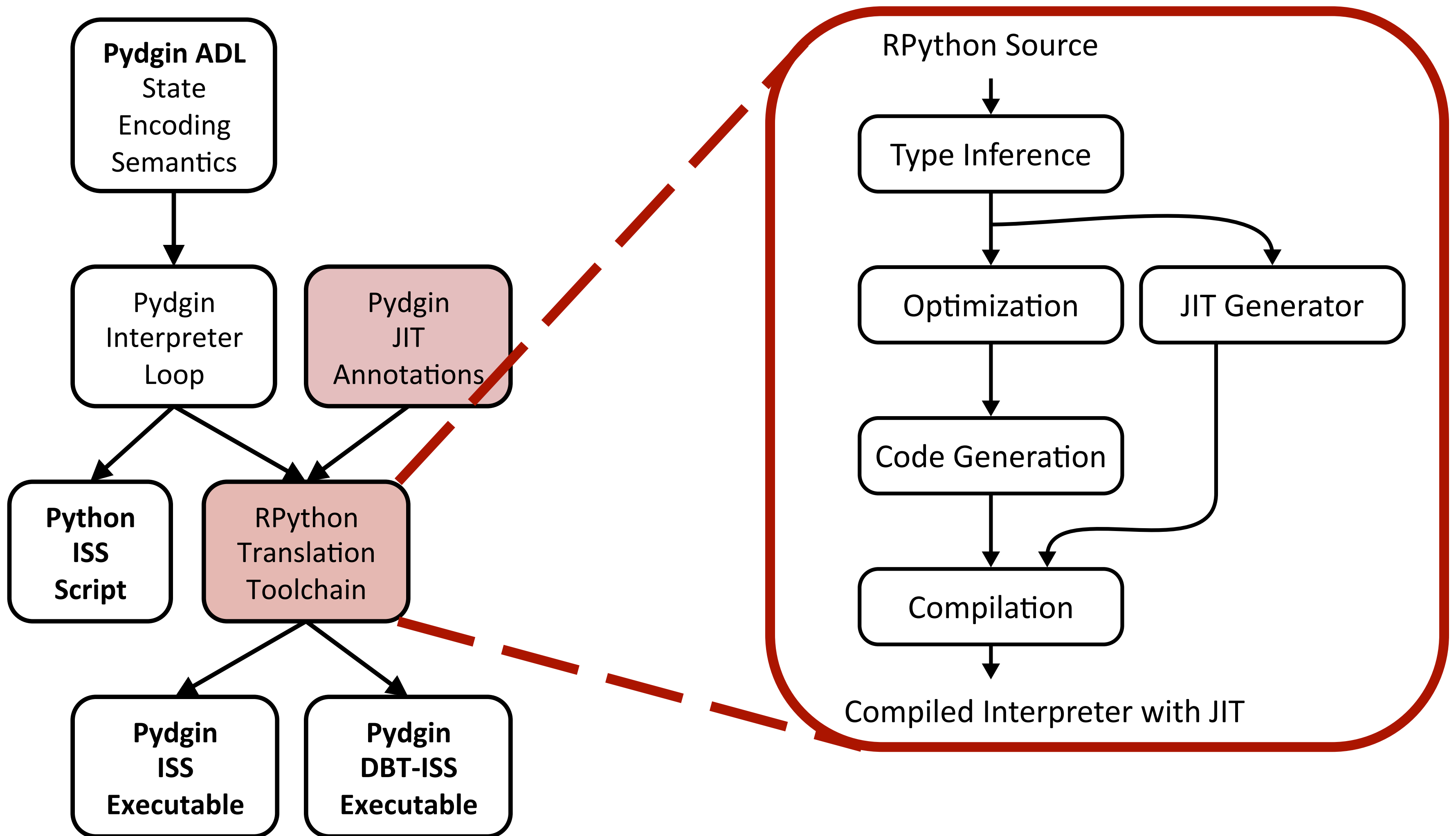

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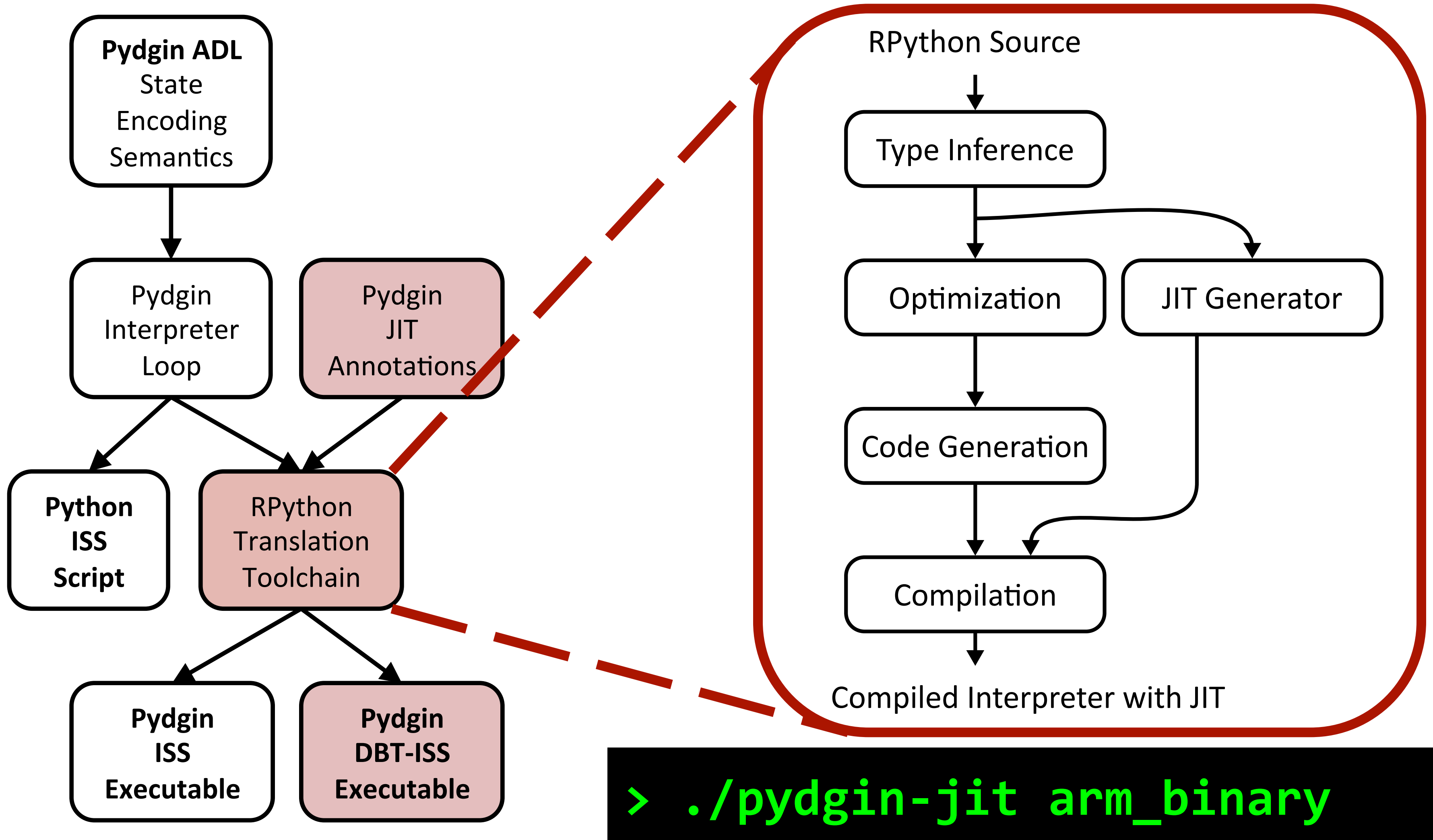
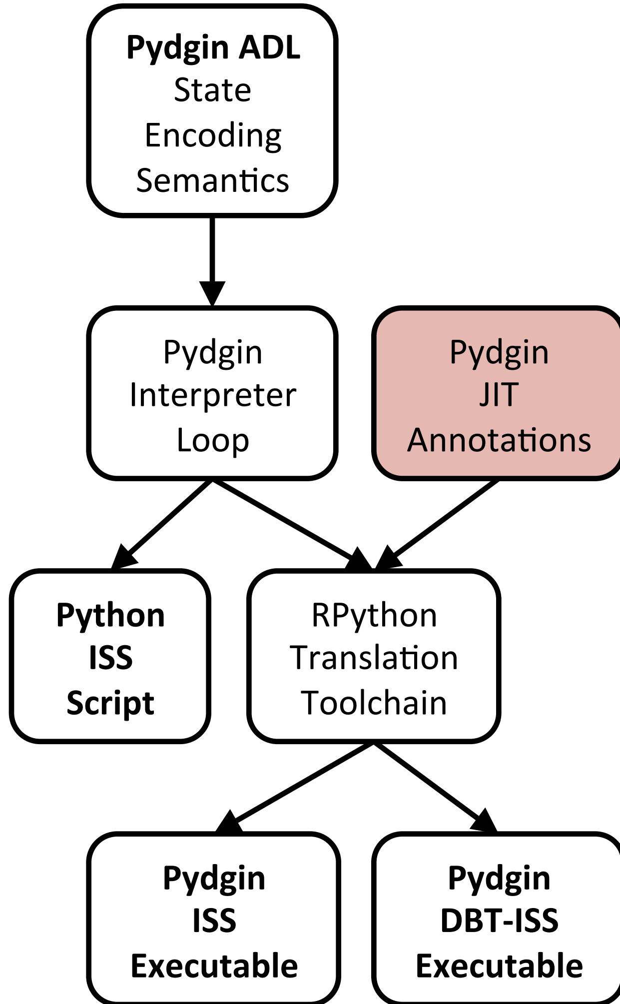


JIT Annotations



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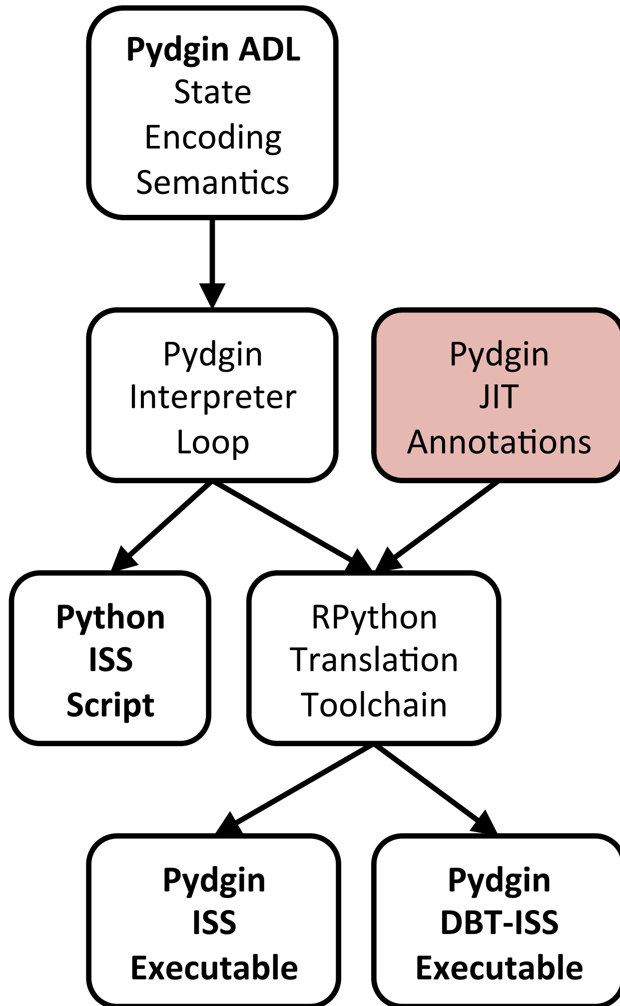
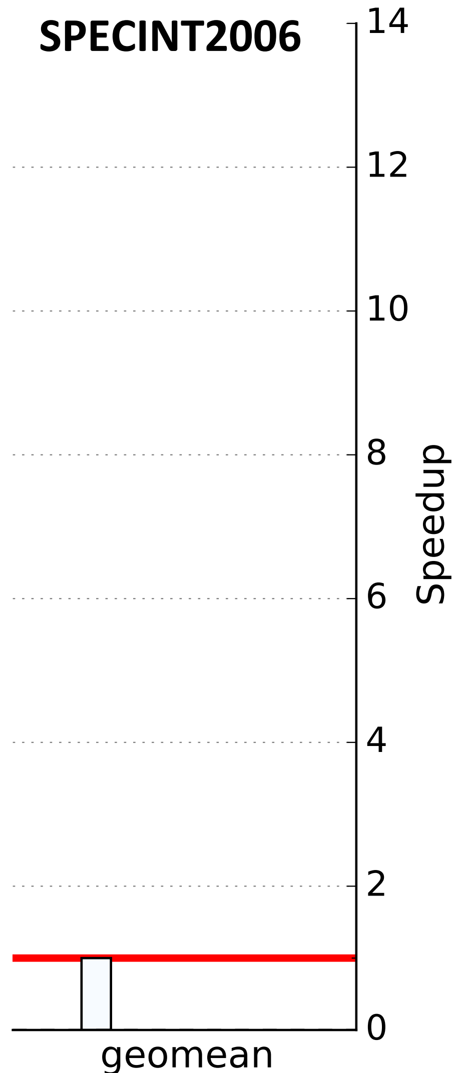


Creating a competitive JIT requires additional RPython JIT hints:

JIT Annotations



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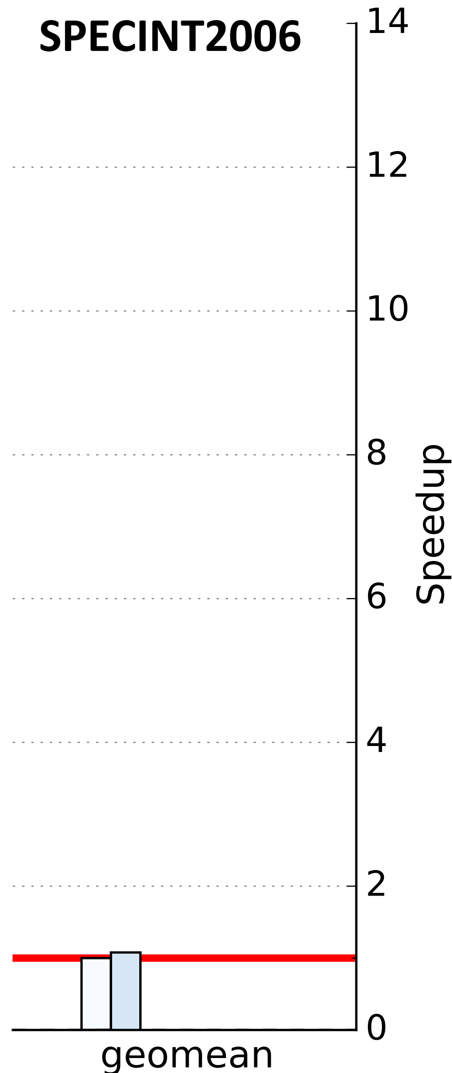
JIT Annotations



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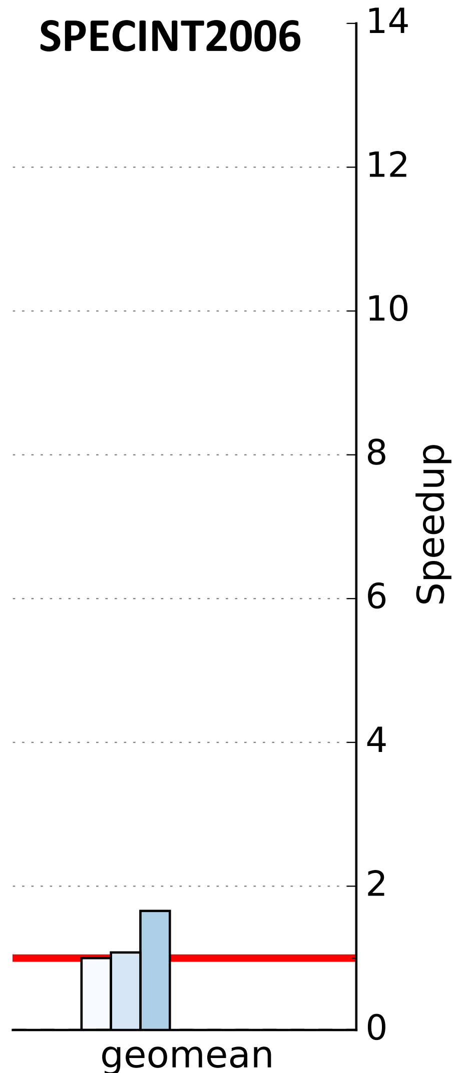
JIT Annotations



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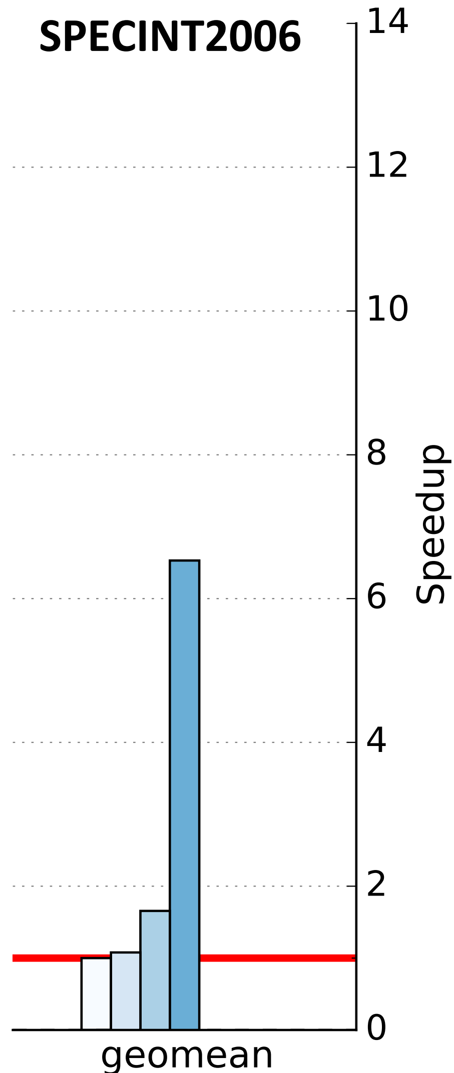

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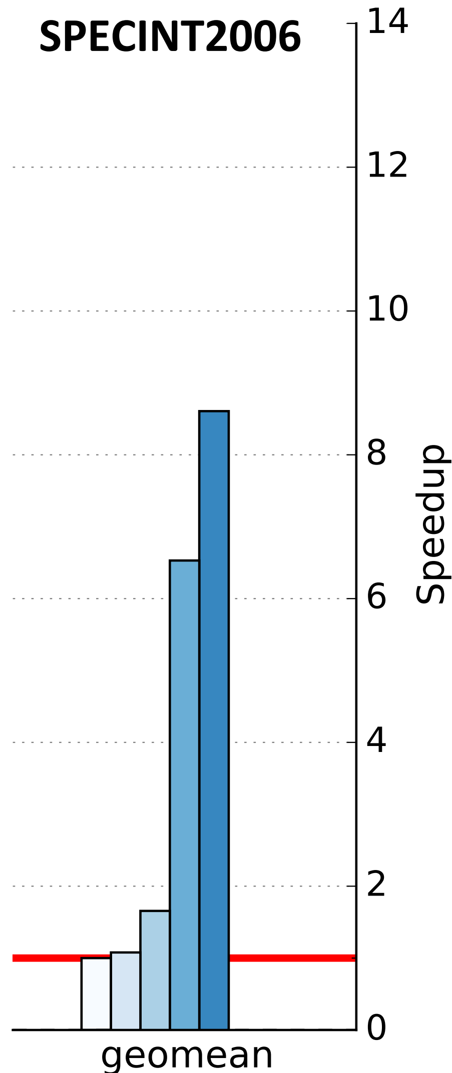

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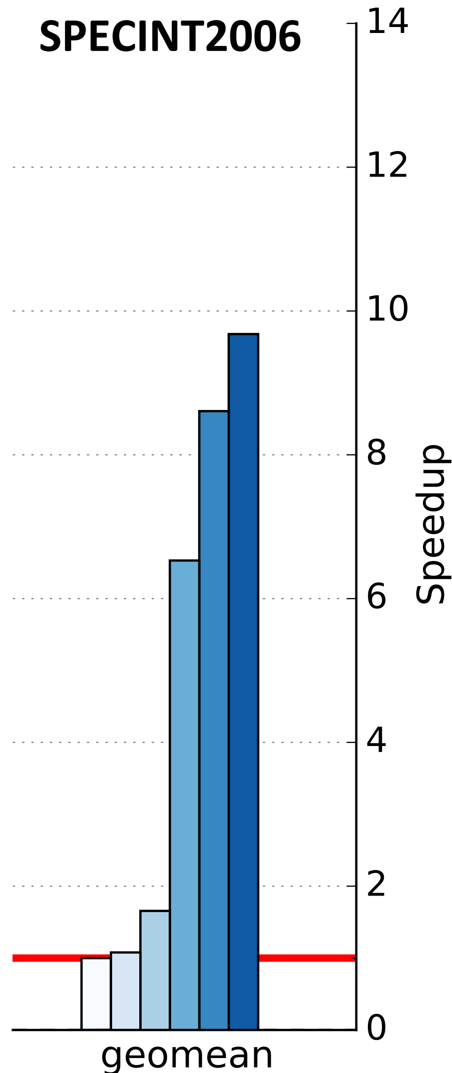

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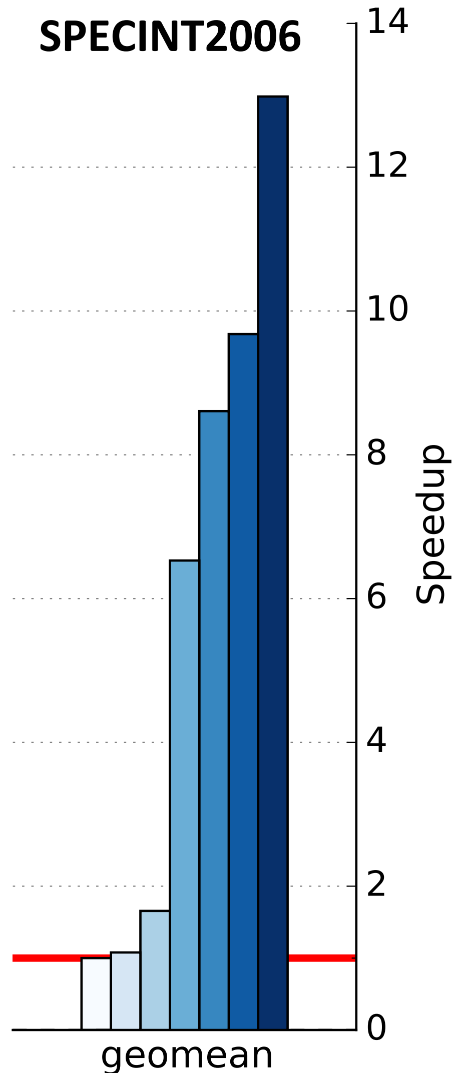

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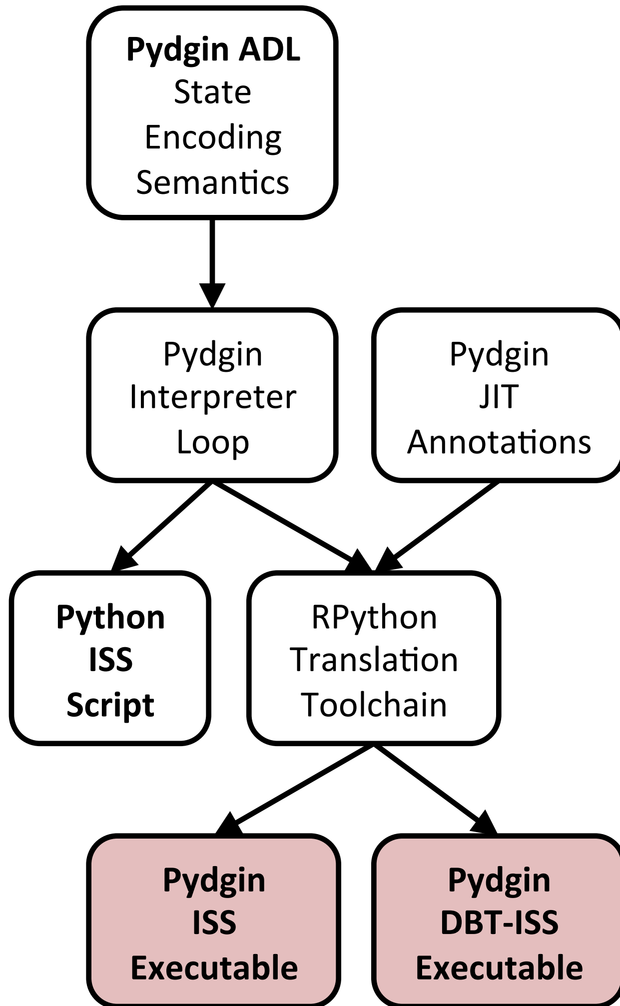
Pydgin ISS Evaluation



Two ISSs implemented in Pydgin

- Simplified-MIPS
- ARMv5

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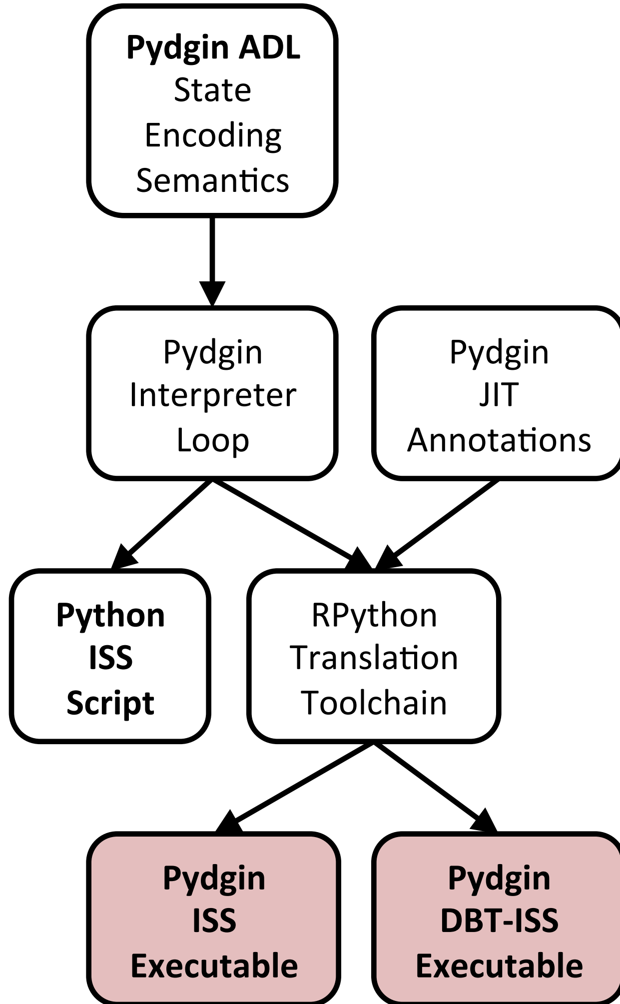

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Simplifications

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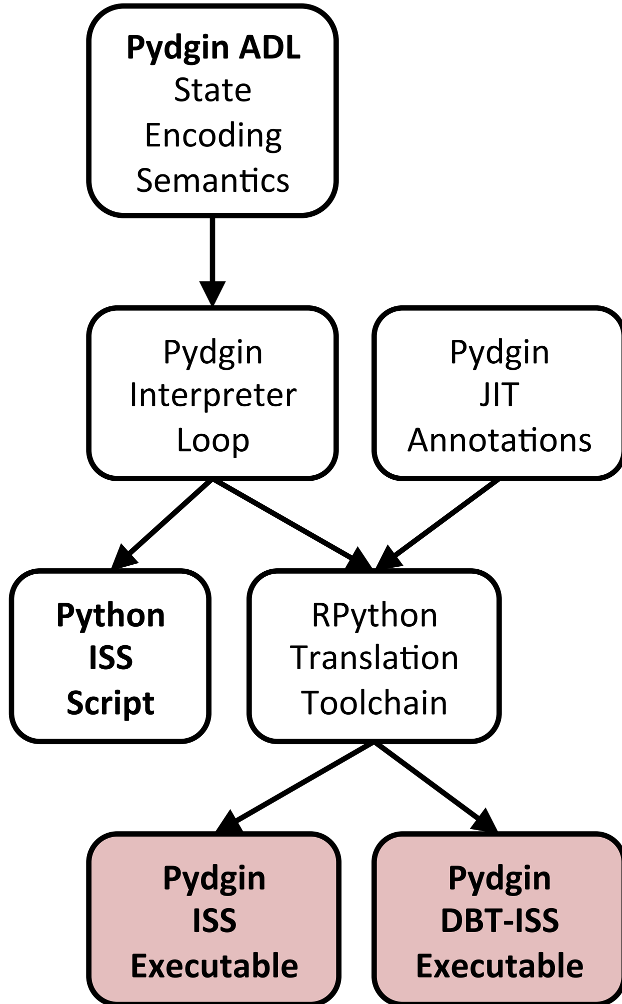

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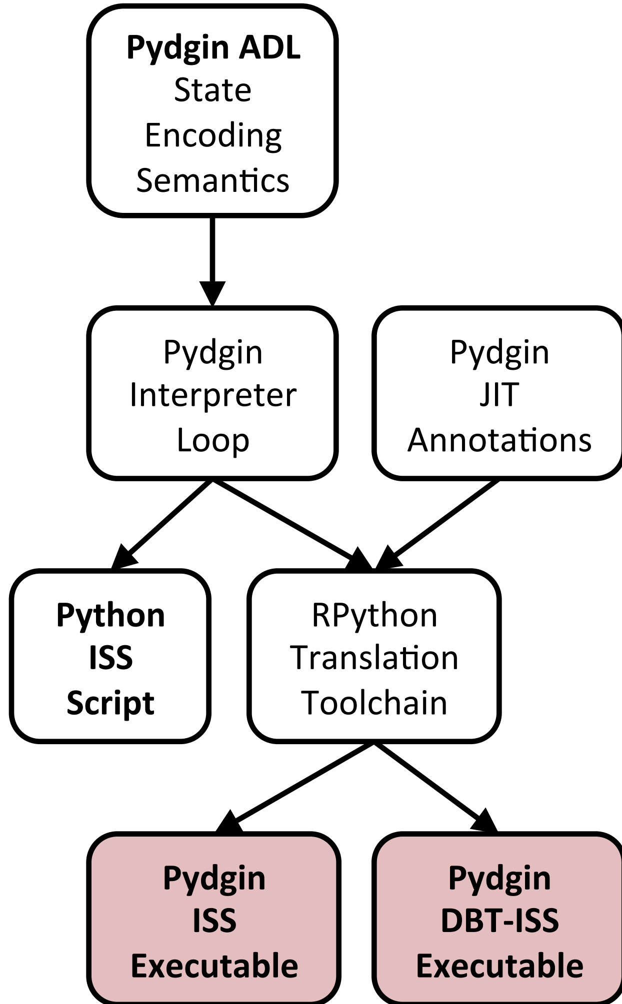

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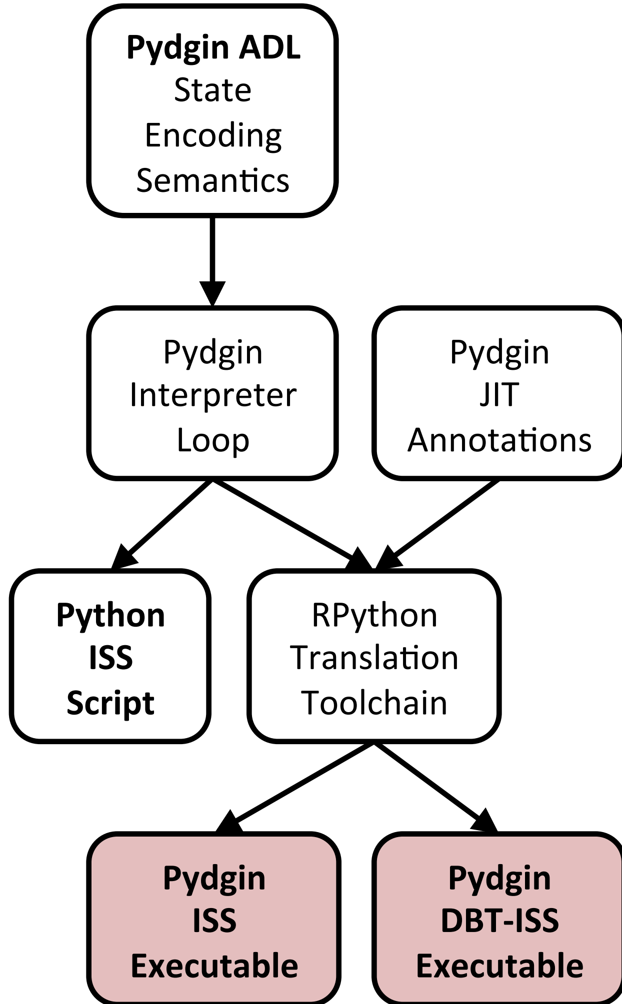

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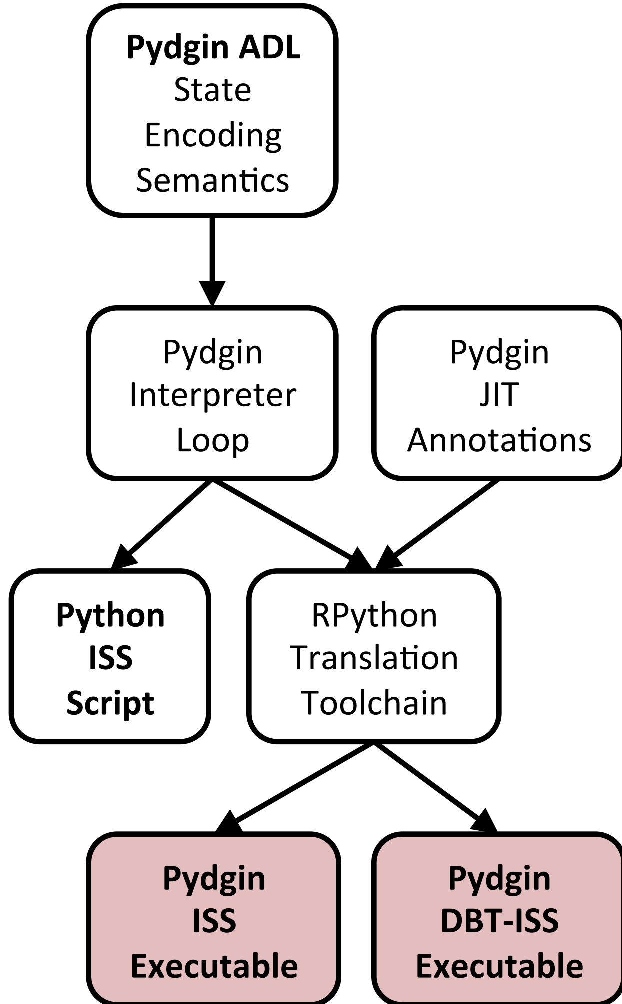

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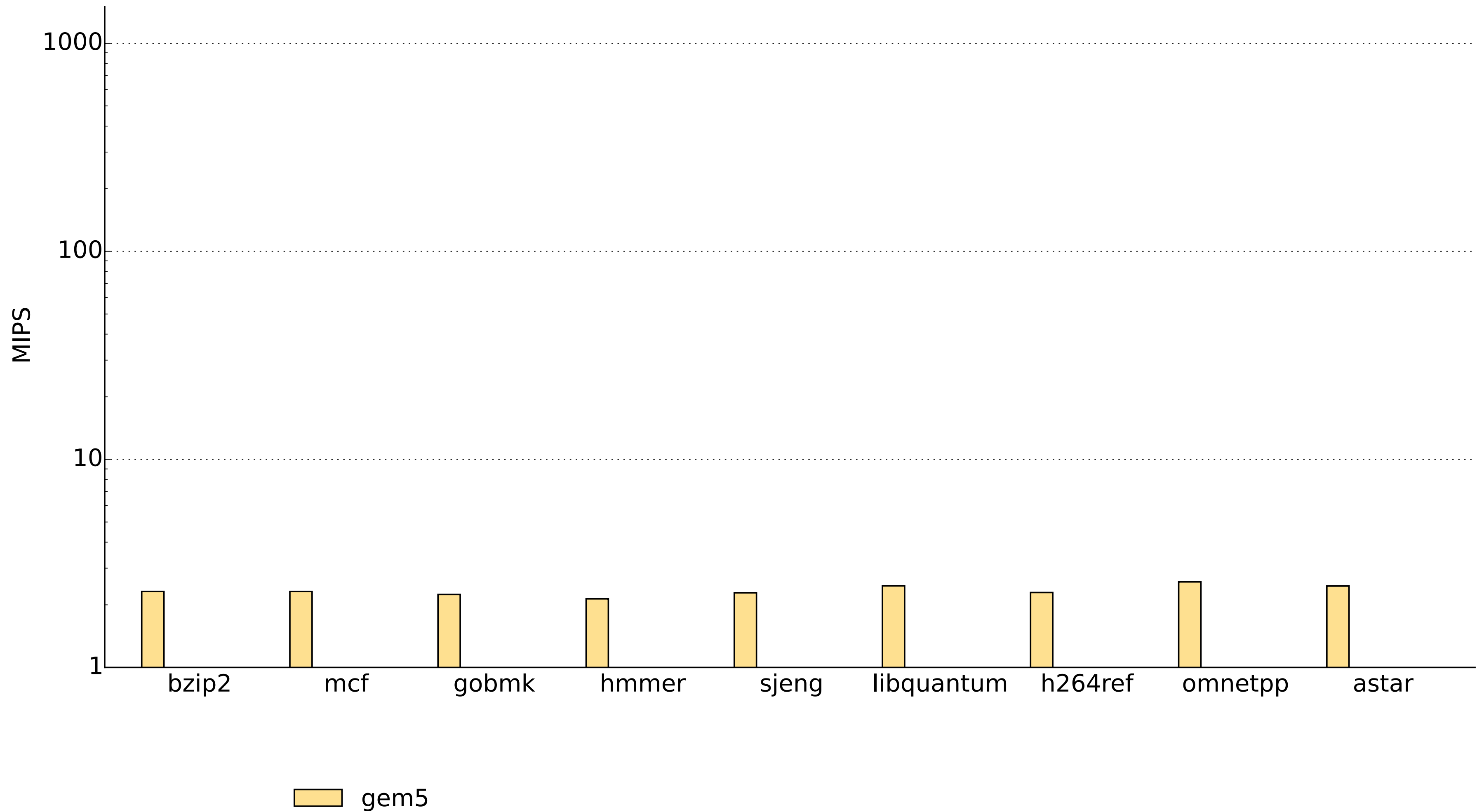
ISS Comparison: ARMv5



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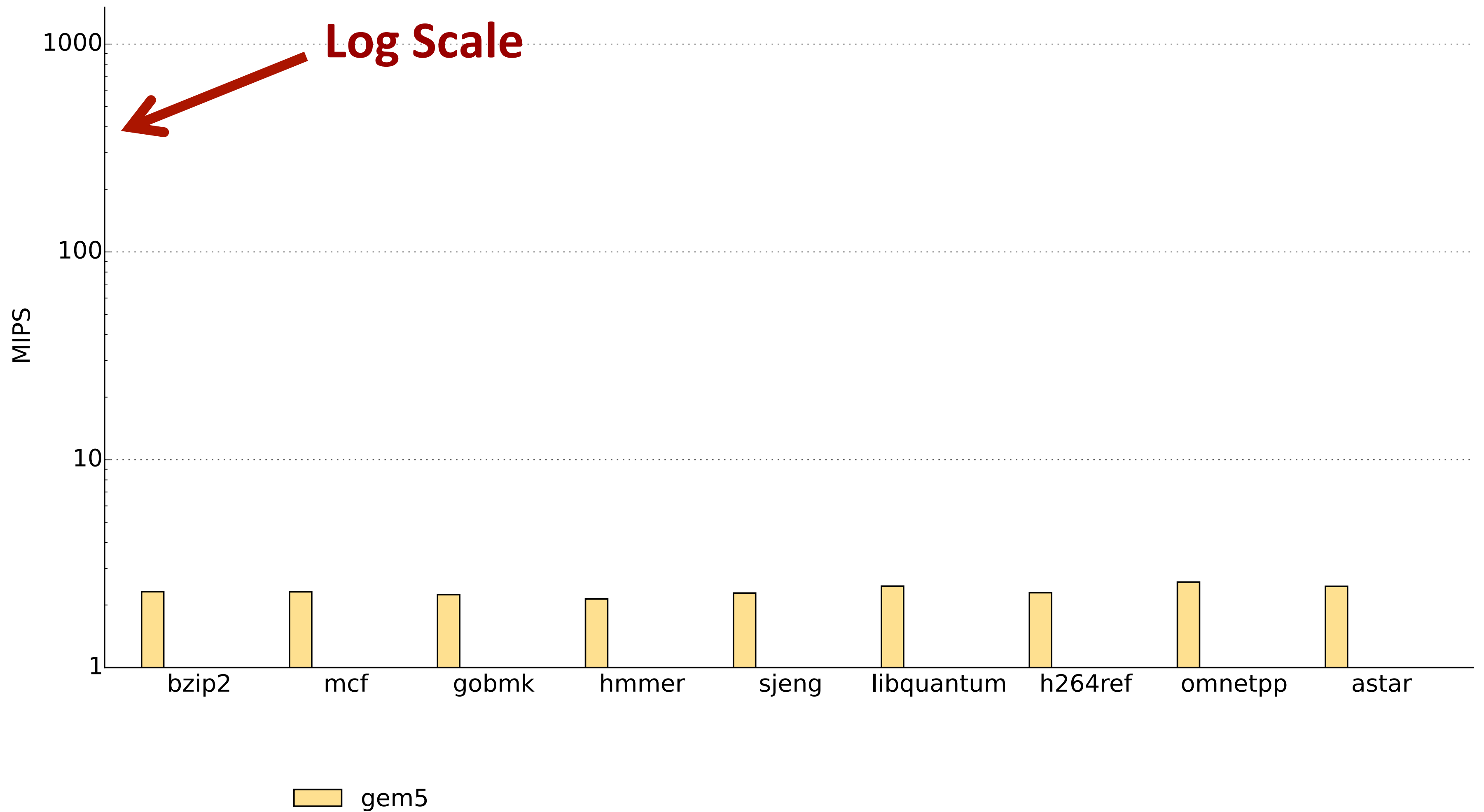

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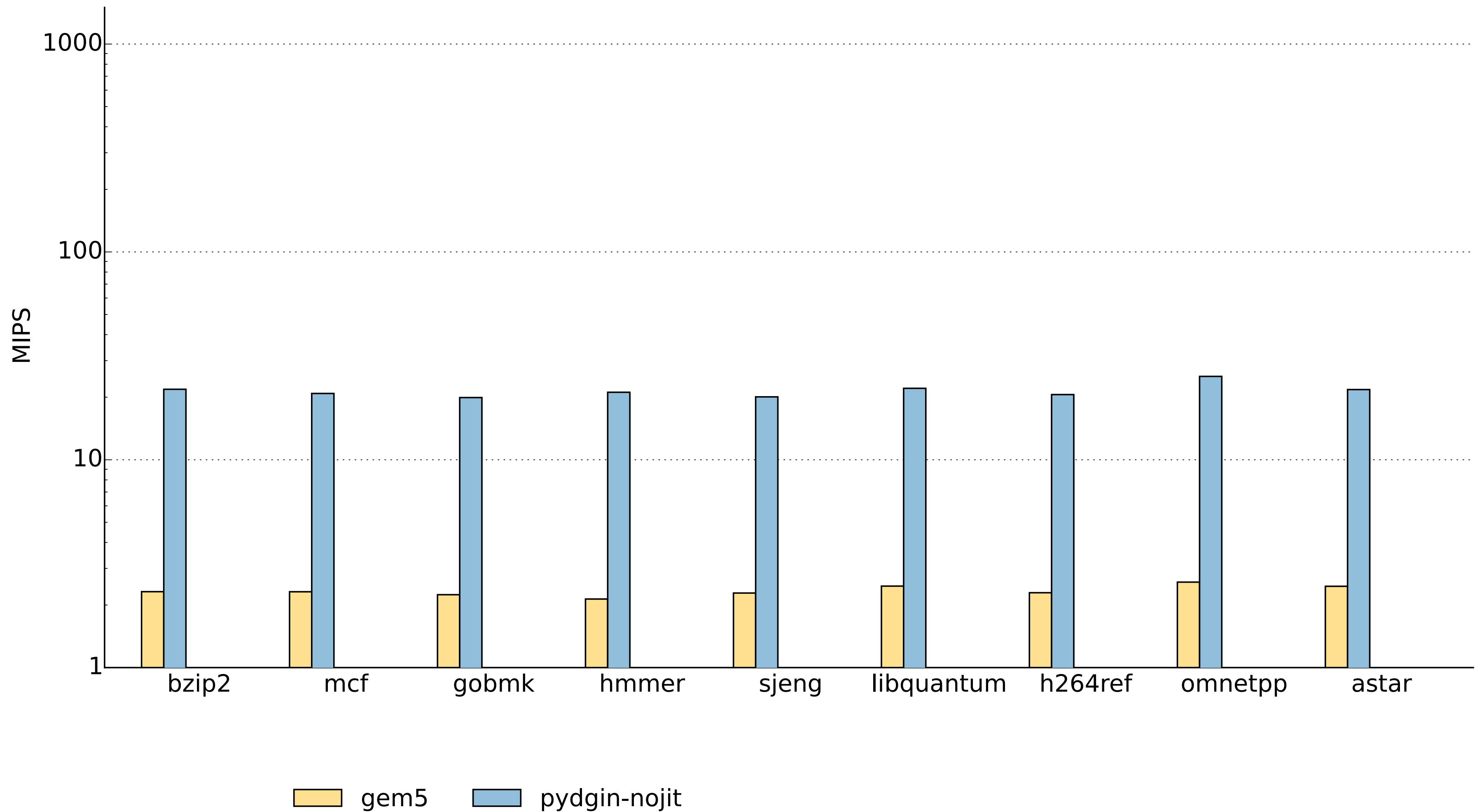

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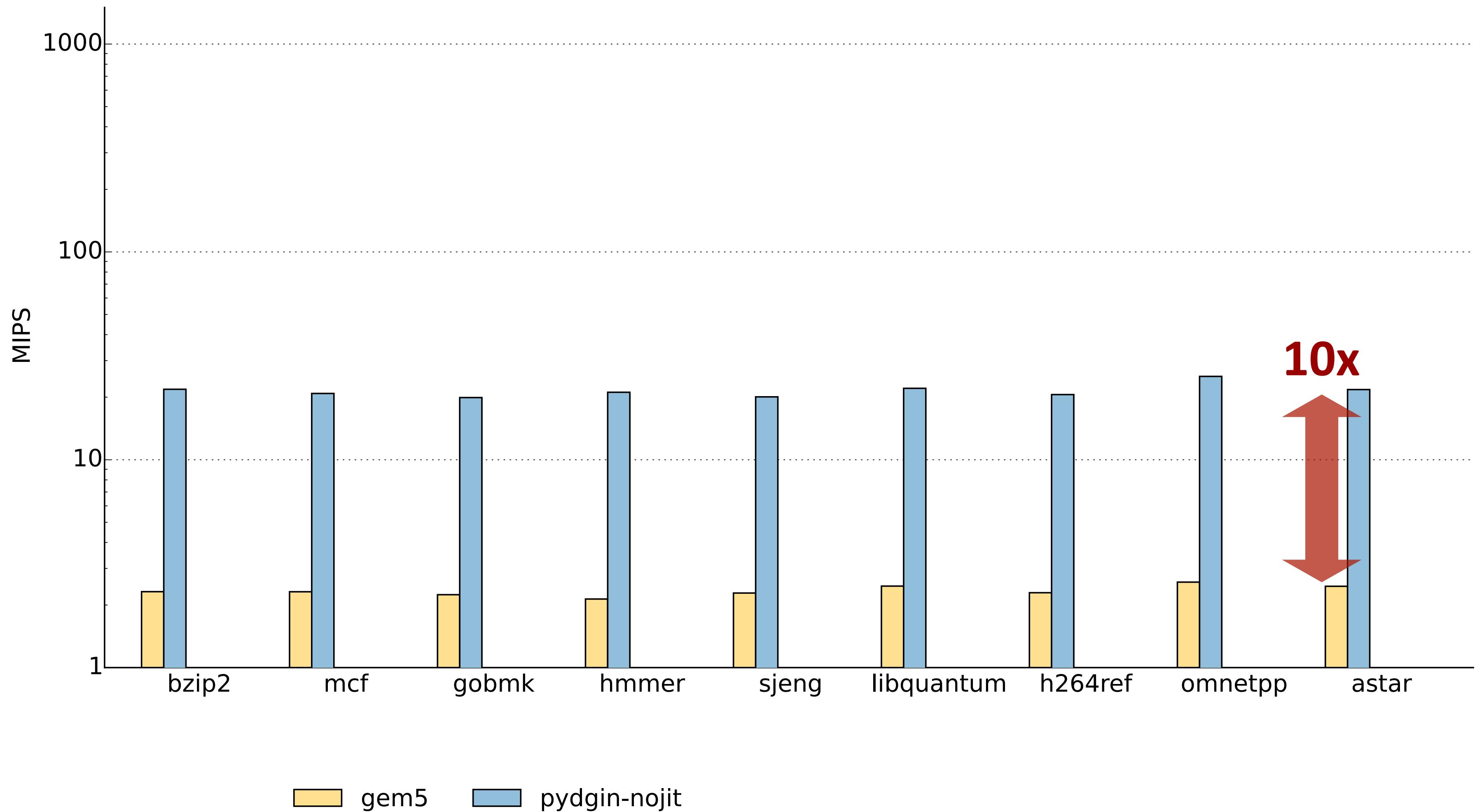

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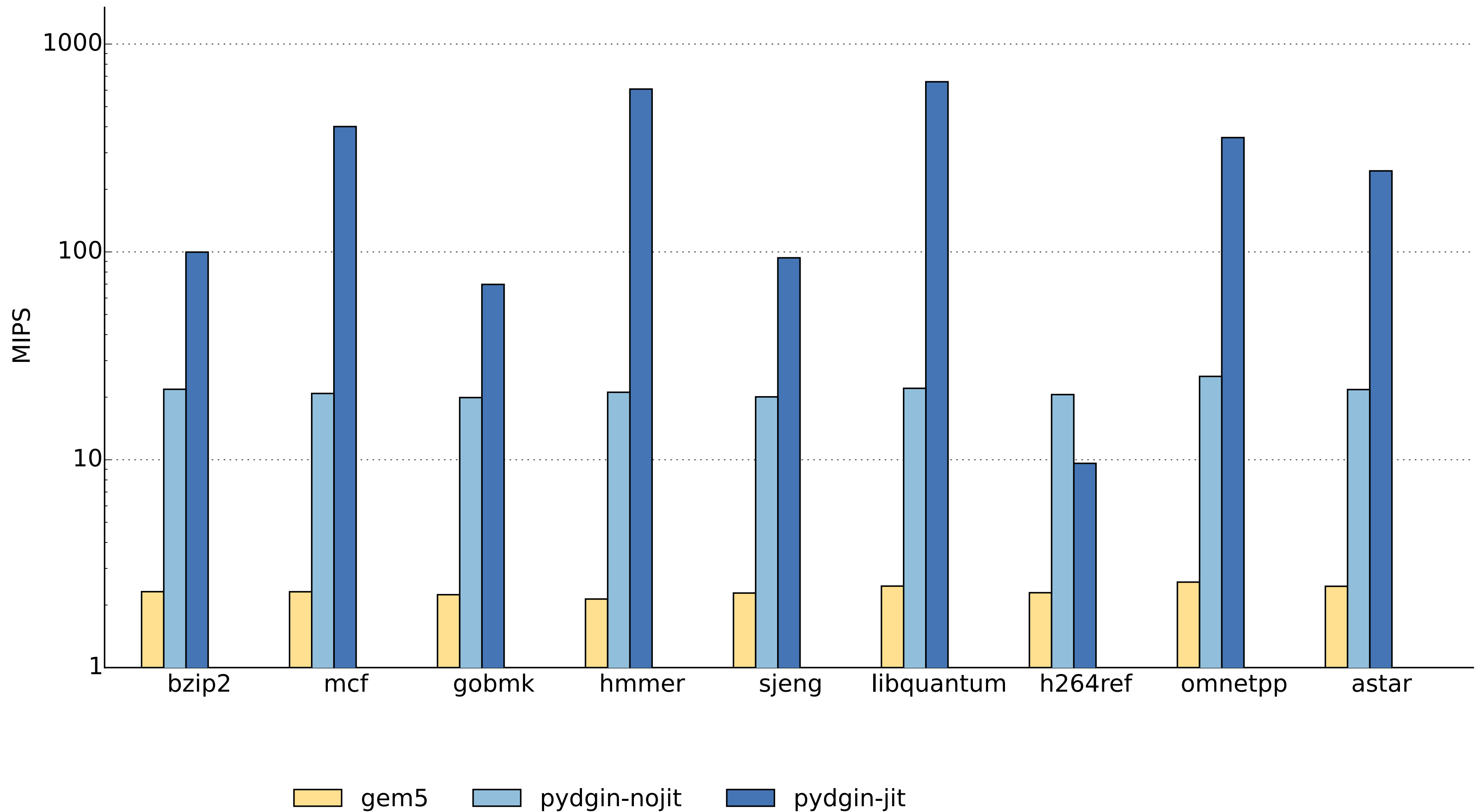

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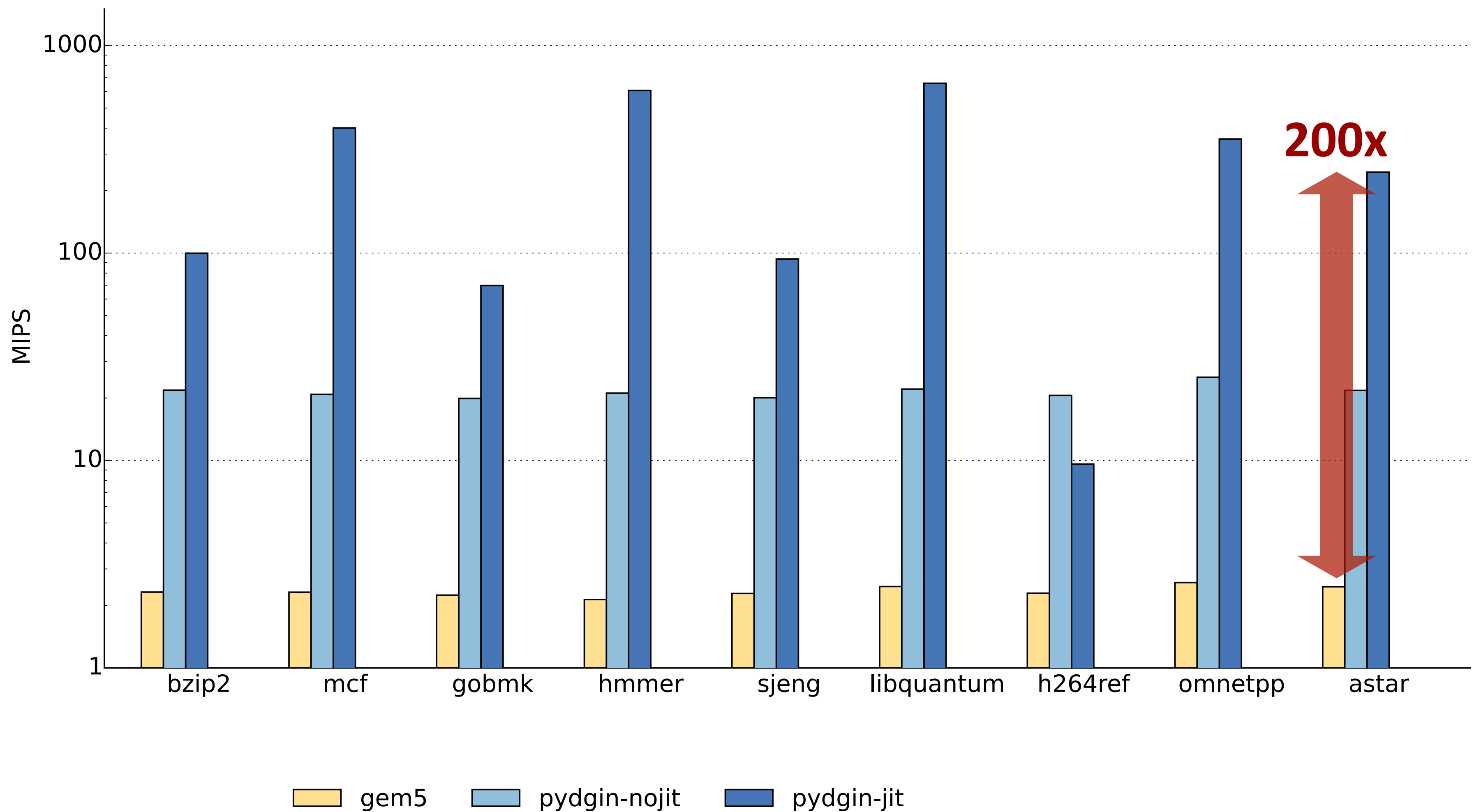

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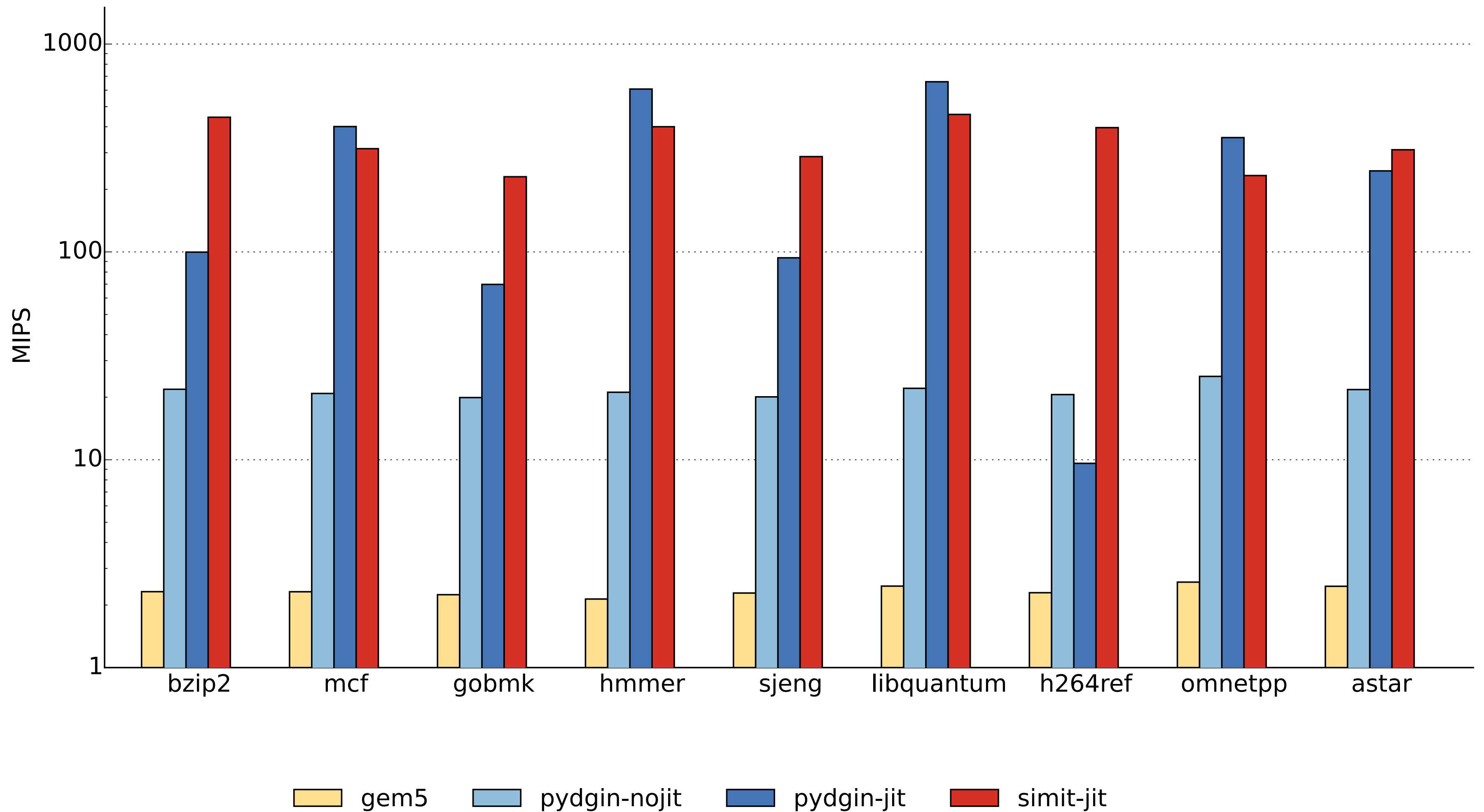

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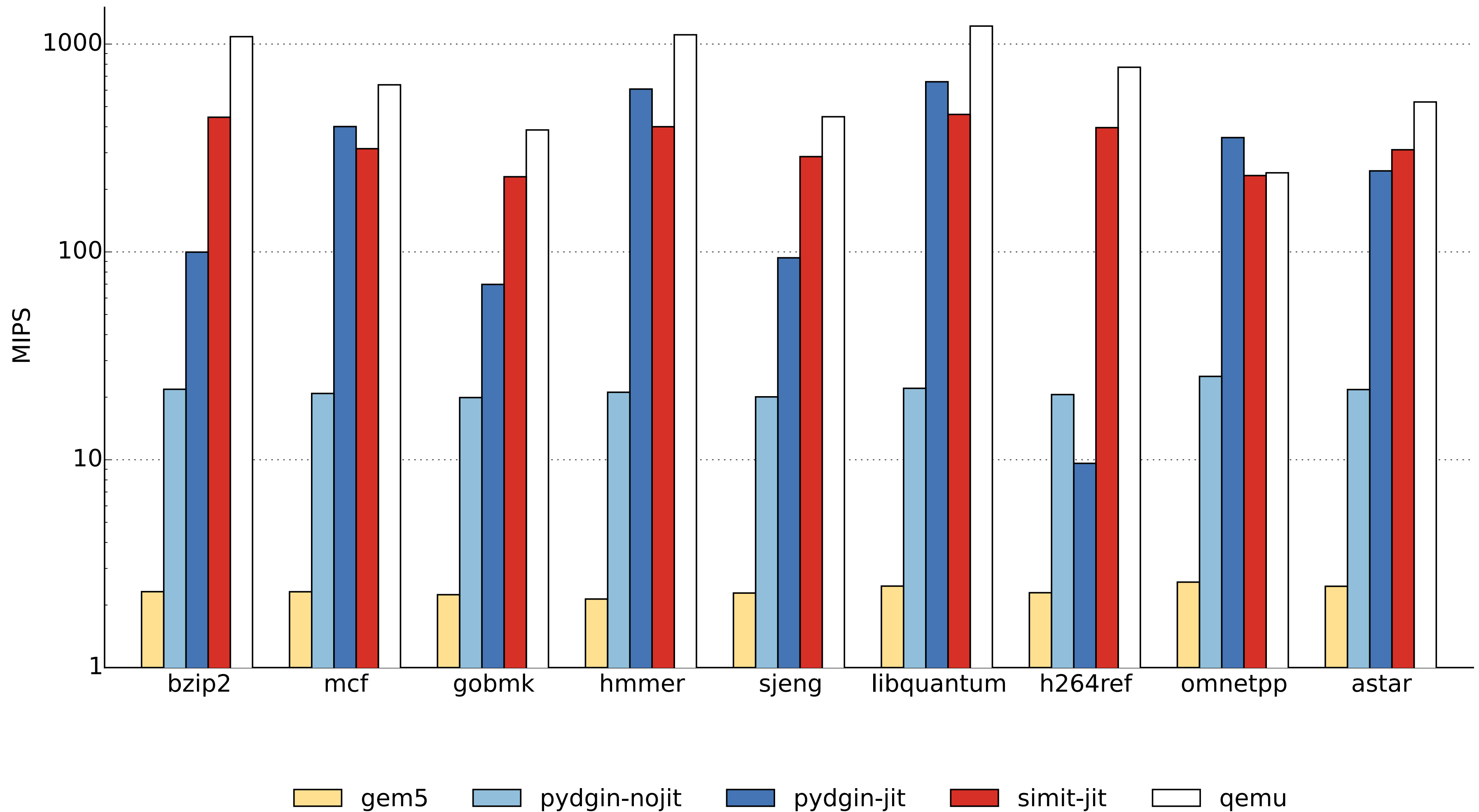

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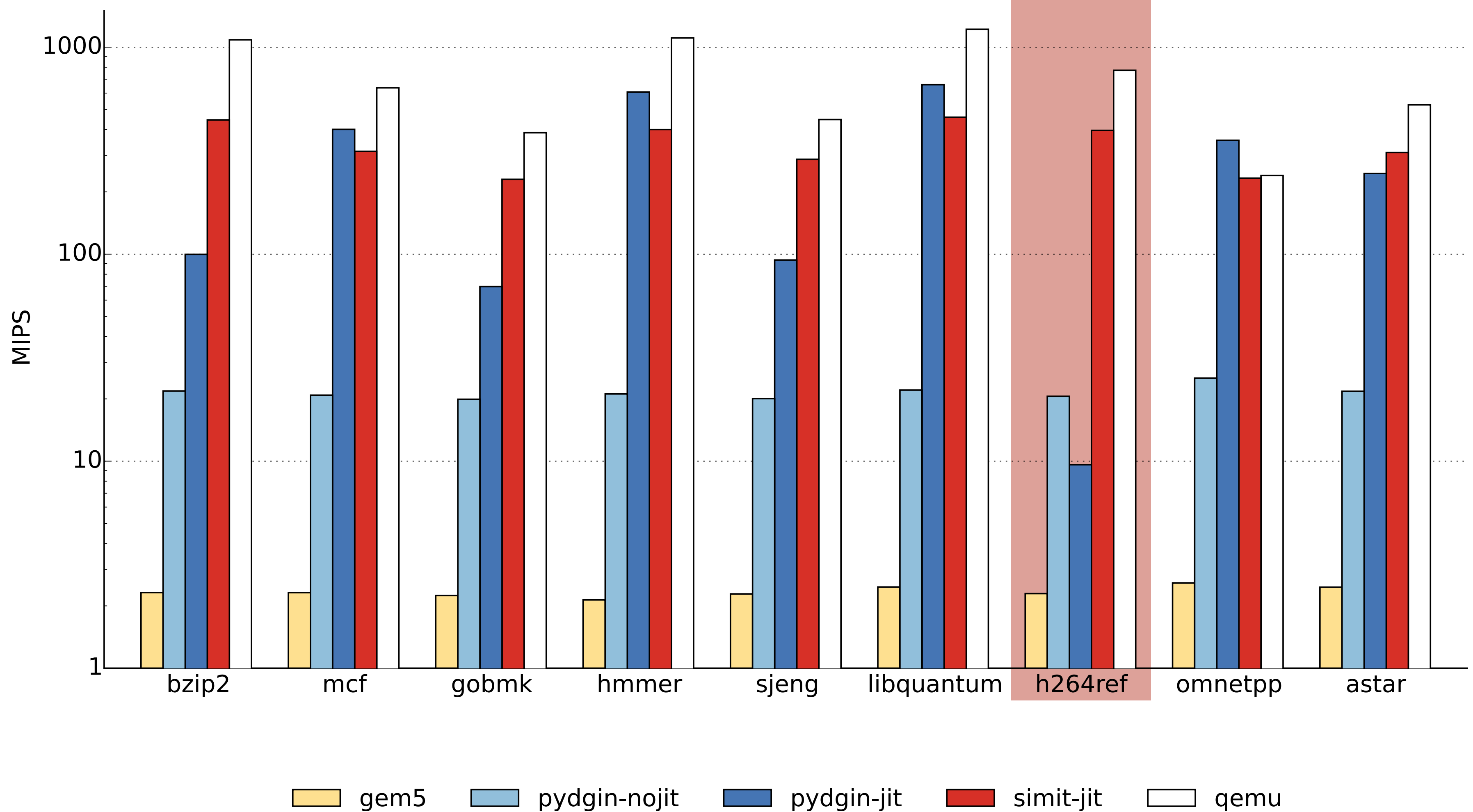

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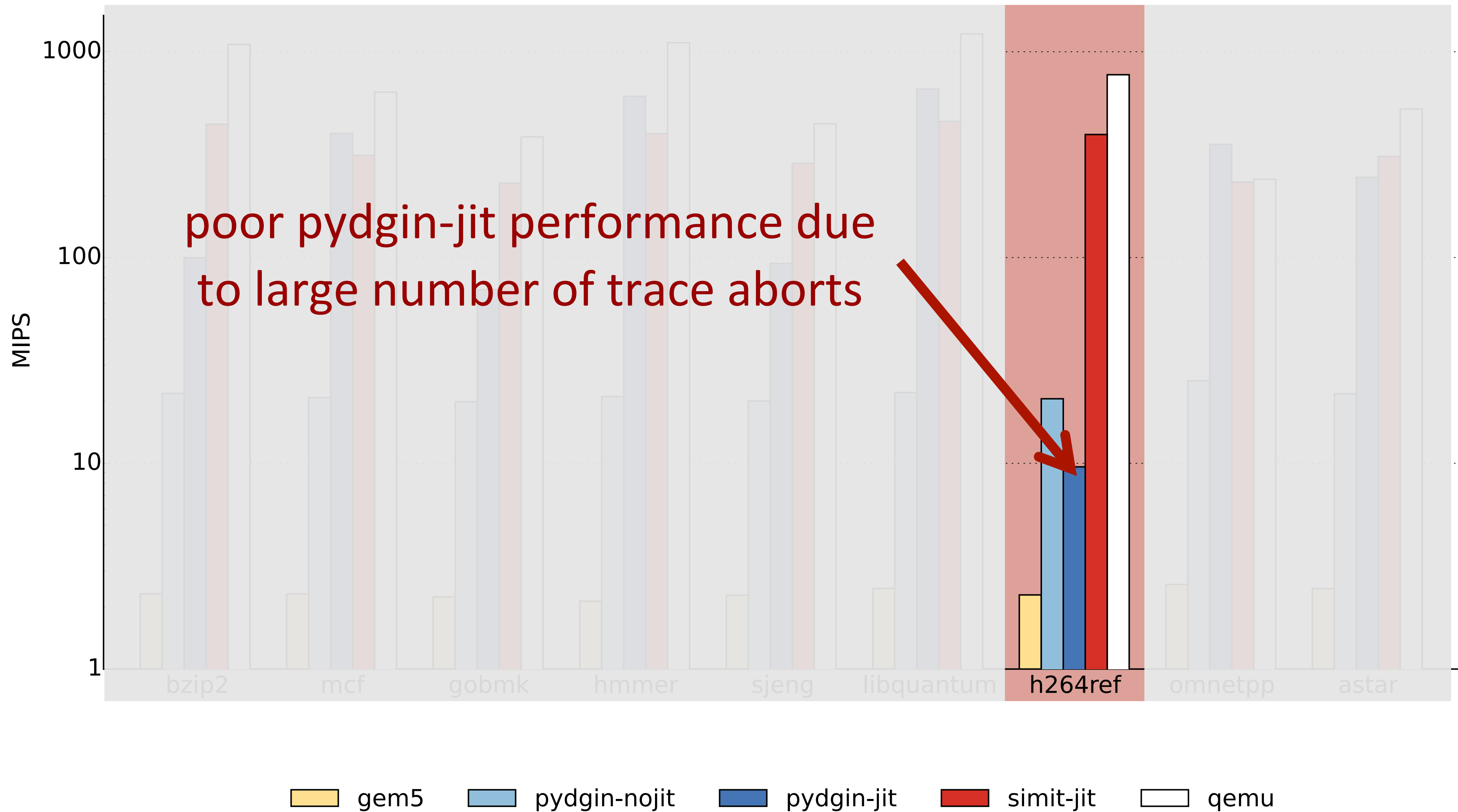

Performance vs. Maximum Trace Length

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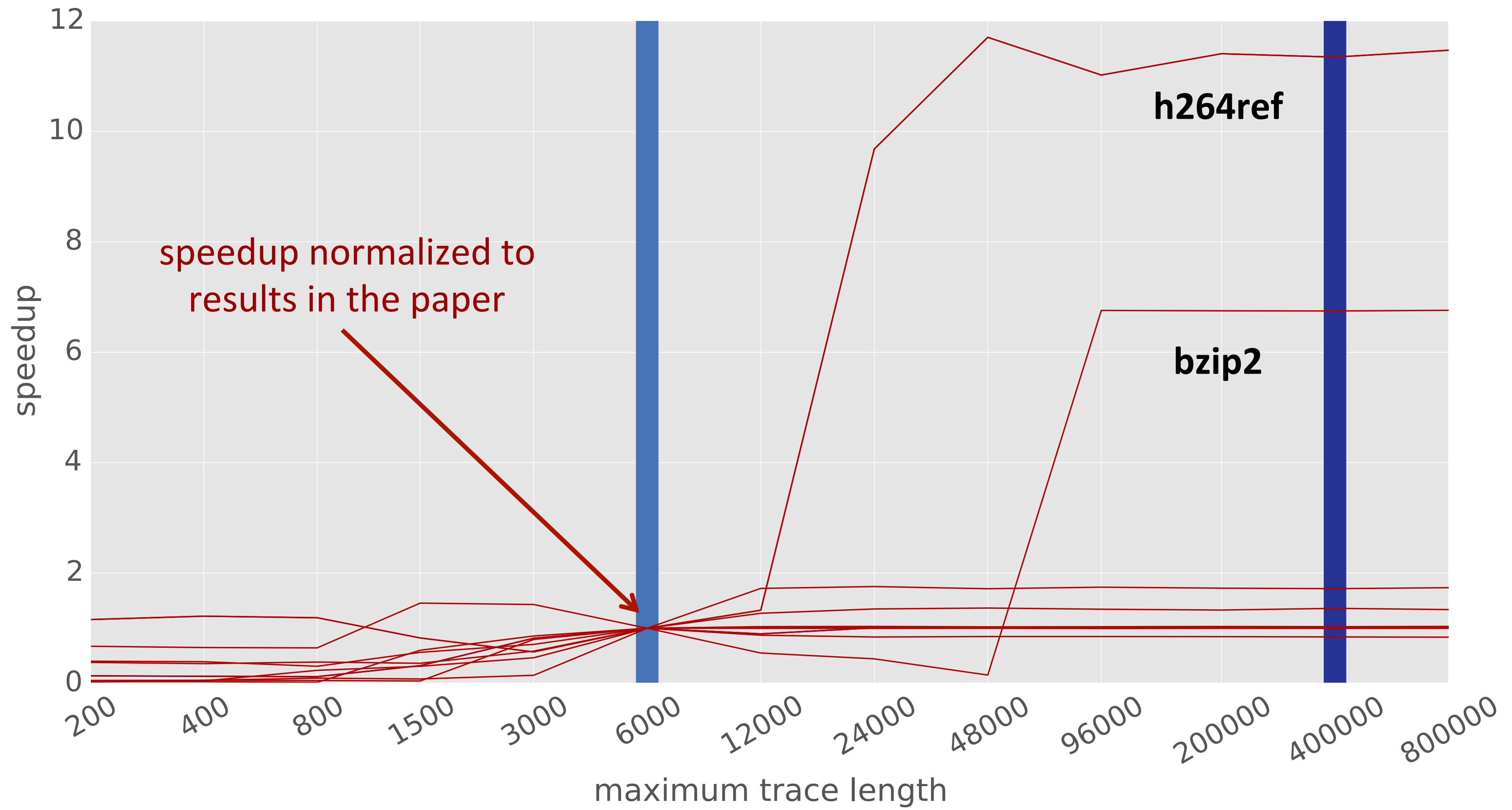
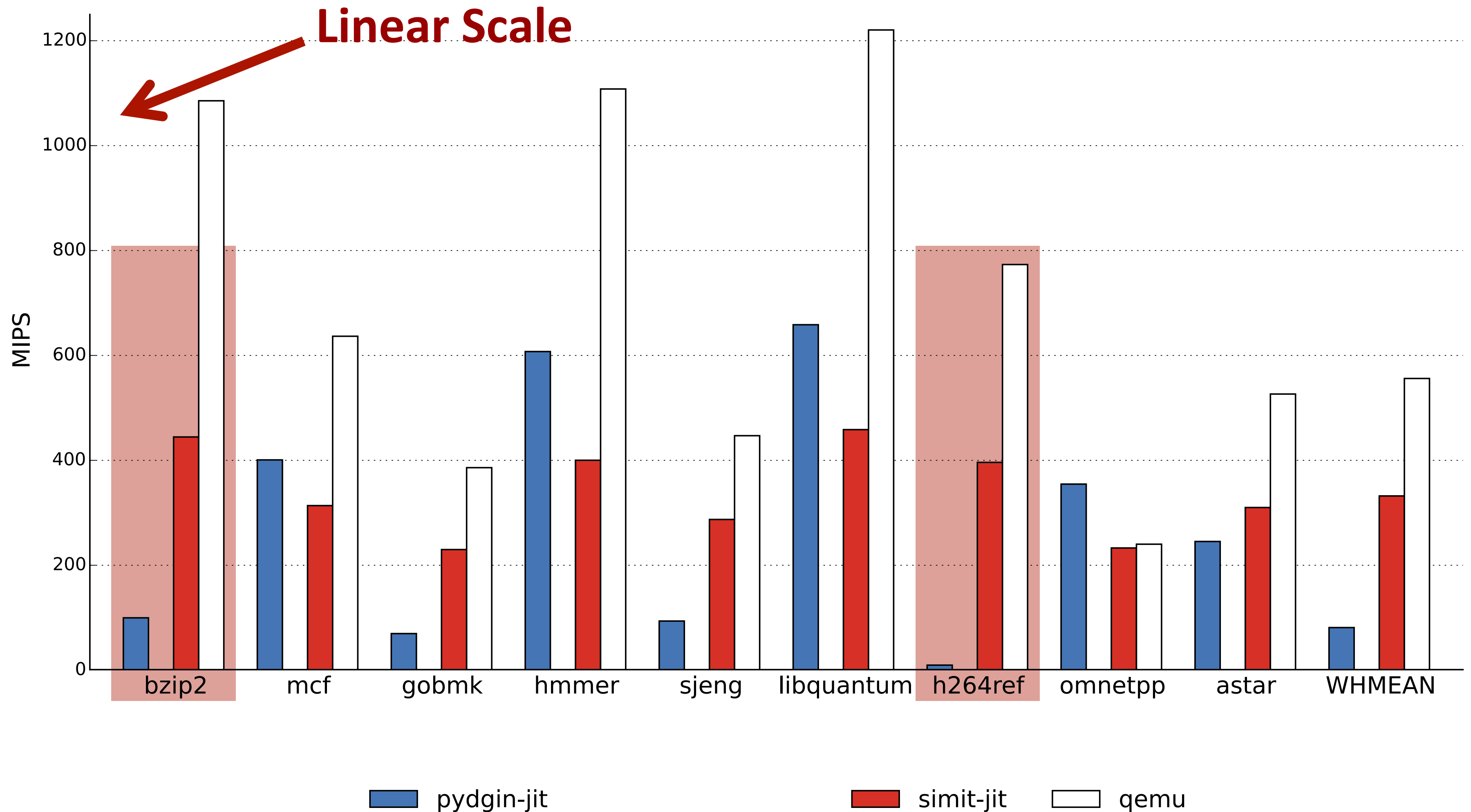


Results: ARM with Longer Traces



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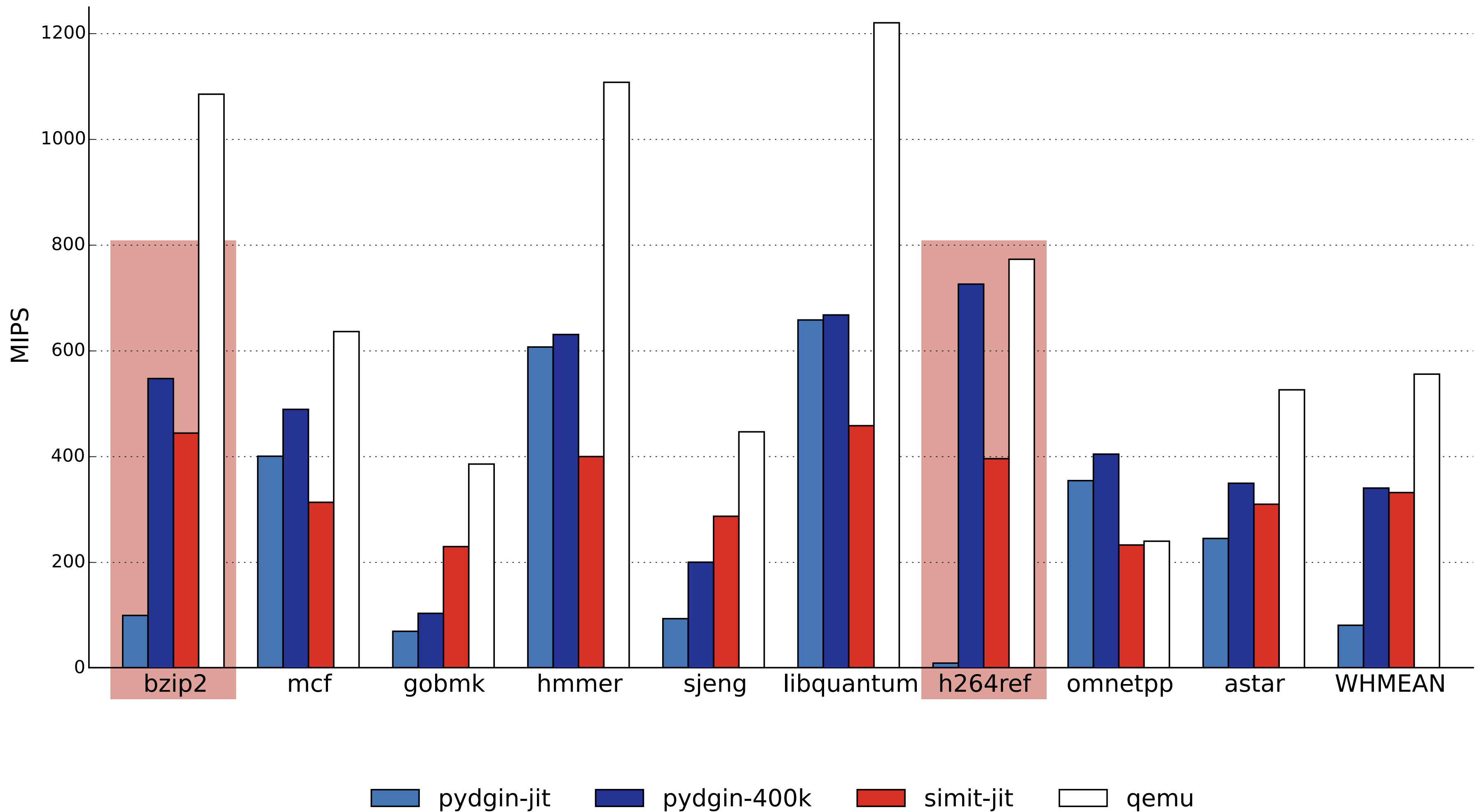

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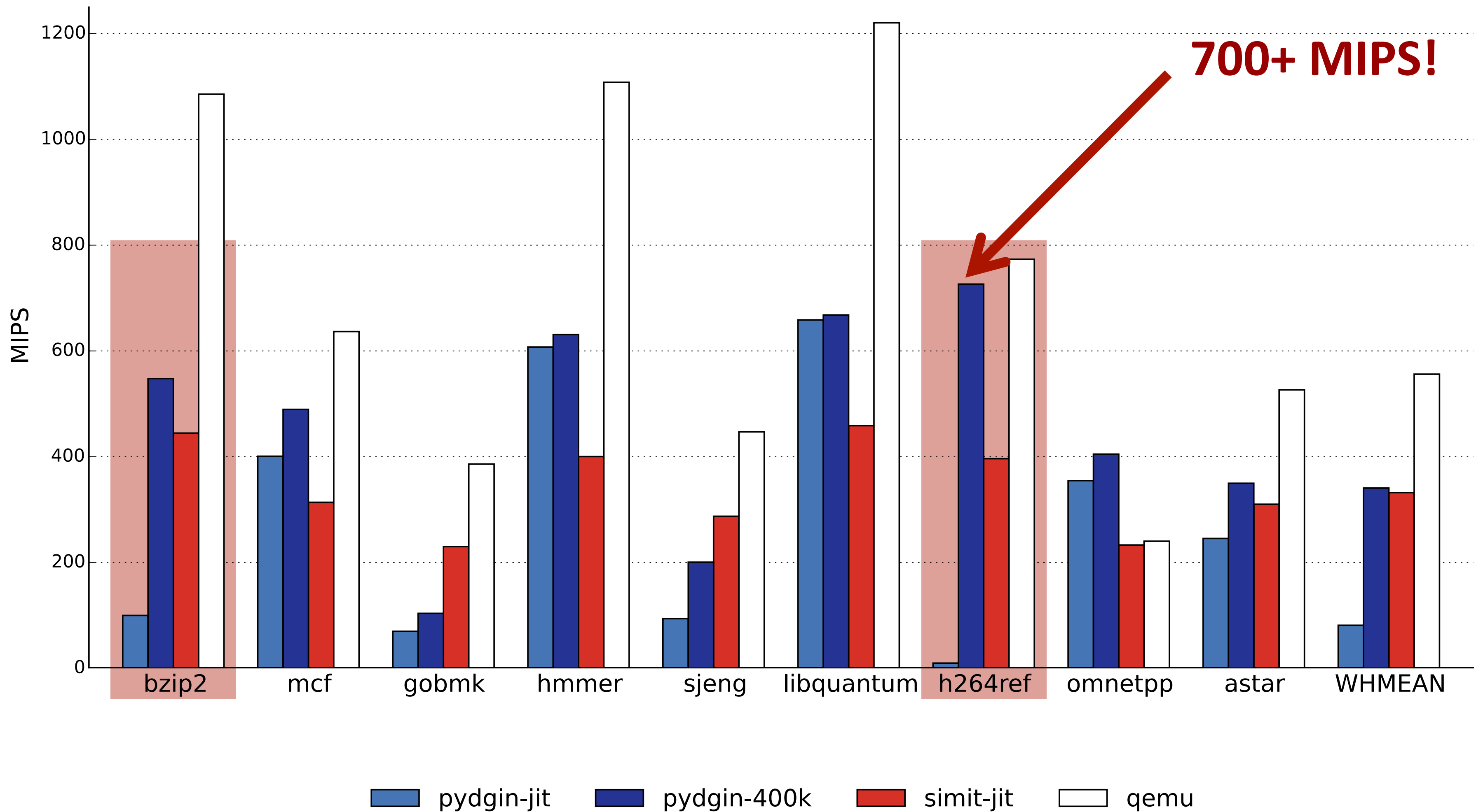

Improving with RPython

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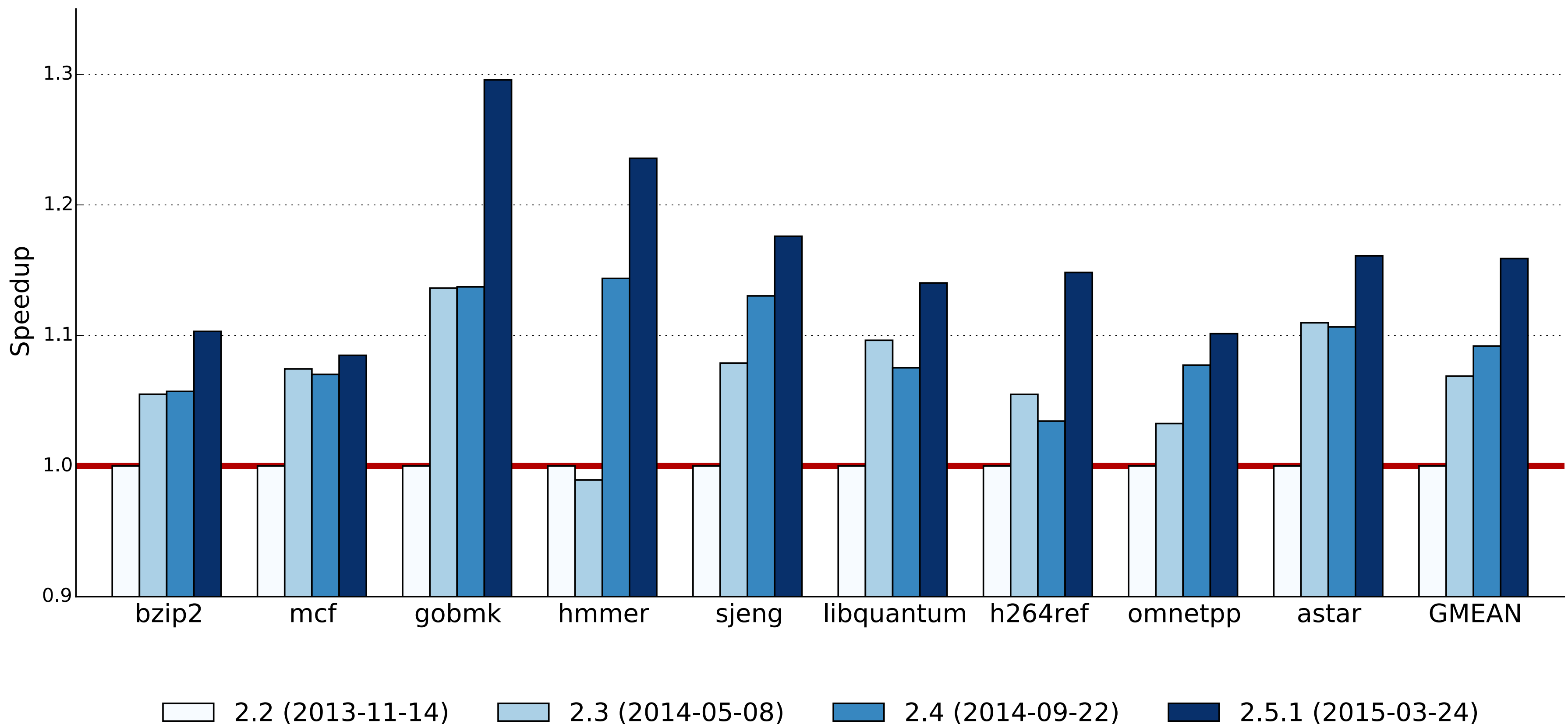

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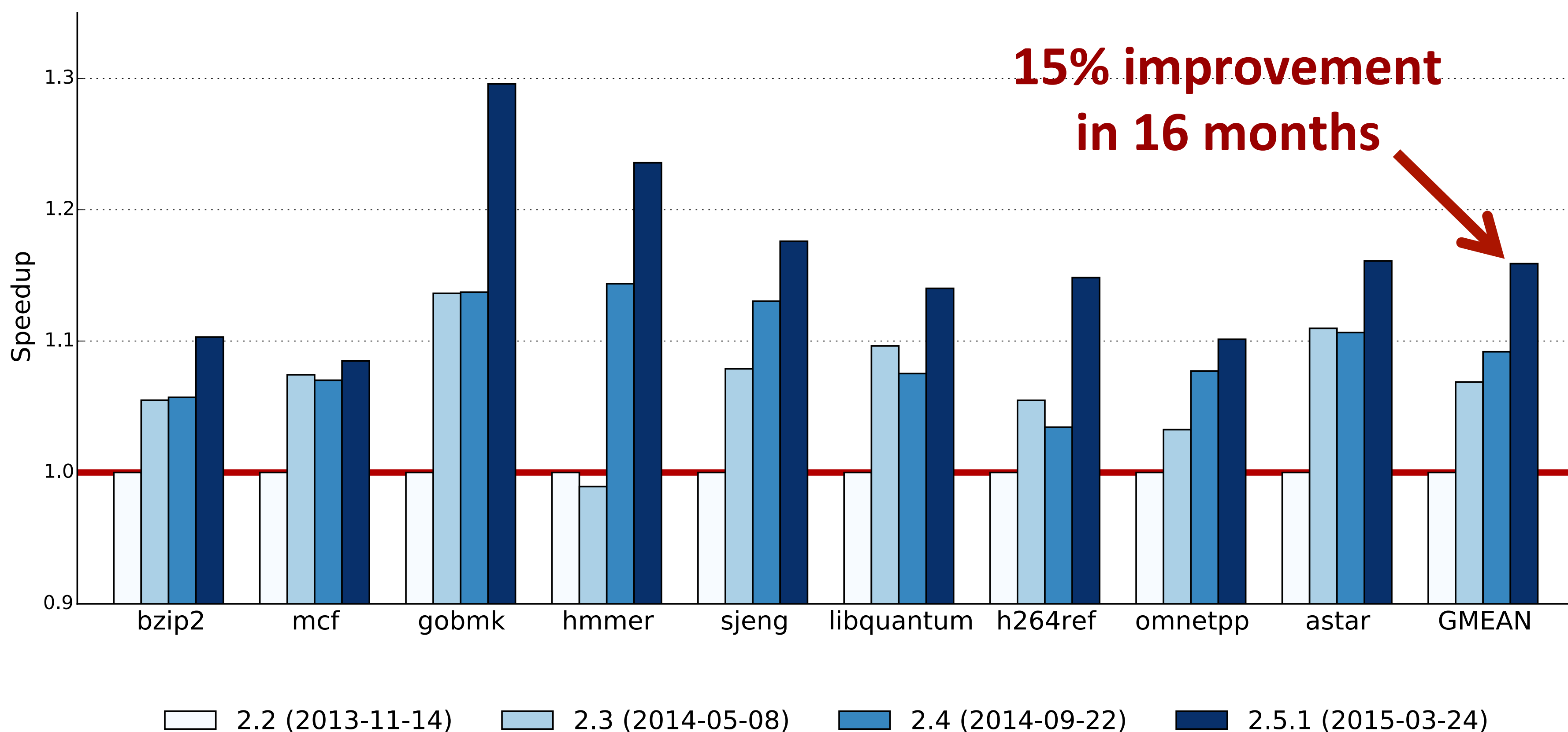

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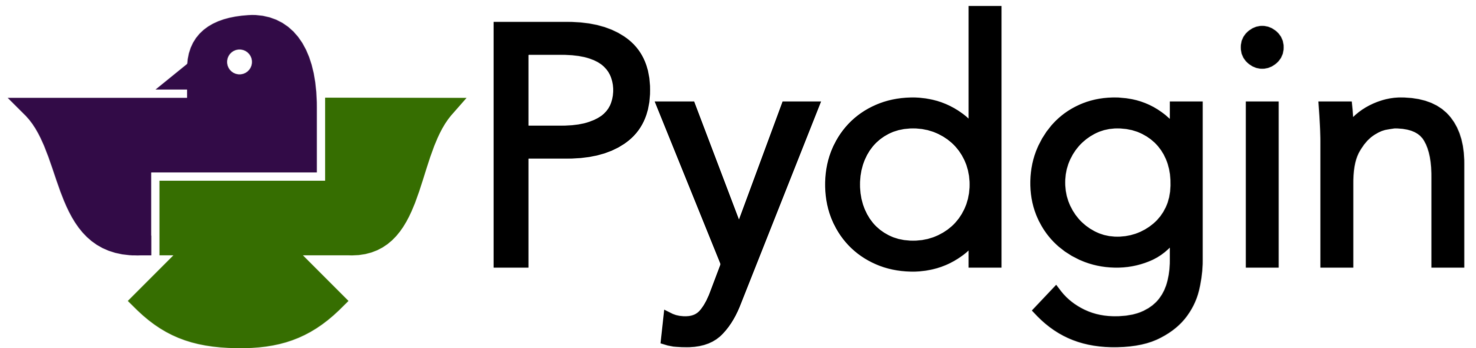
Many opportunities for future improvements:

- more features and ISA implementations
- performance optimizations

Conclusion

Pydgin is a productive, **open-source** Python framework for creating fast instruction set simulators.



https://github.com/cornell-brg/pydgin

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