# Major Information Session ECE: Computer Engineering

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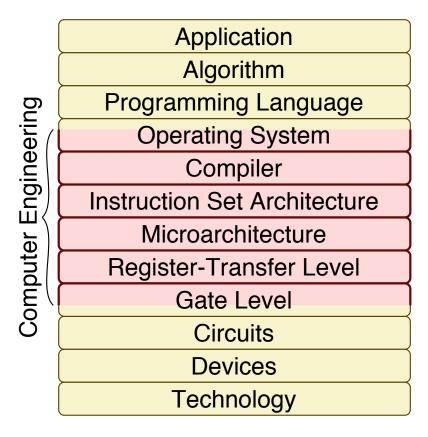
# **The Computer Systems Stack**

#### **Application**

Gap too large to bridge in one step (but there are exceptions, e.g., a magnetic compass)

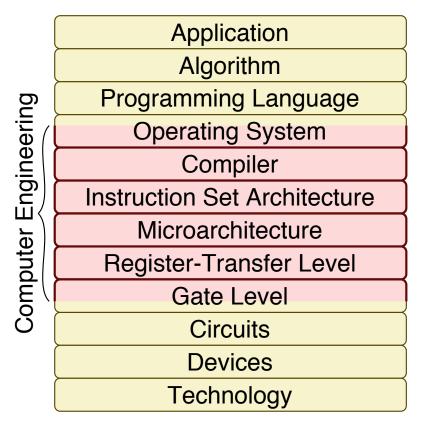
**Technology** 

# **The Computer Systems Stack**



In its broadest definition, computer engineering is the development of the abstraction/implementation layers that allow us to execute information processing applications efficiently using available manufacturing technologies

# CS vs. Computer Engineering vs. EE



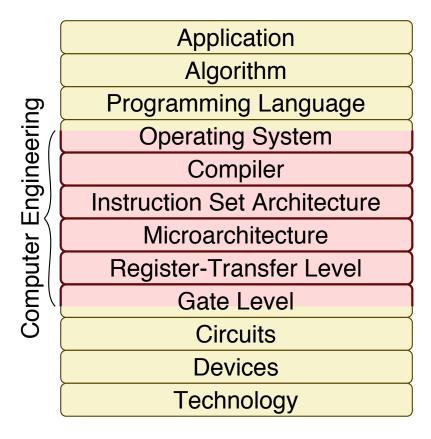
Traditional Computer Science

**Computer Engineering** is at the interface between hardware and software and considers the entire system

Traditional Electrical Engineering

In its broadest definition, computer engineering is the development of the abstraction/implementation layers that allow us to execute information processing applications efficiently using available manufacturing technologies

# Computer Engineering: From C/C++ to Logic Gates



#### **C/C++ Programming Language**

```
template < typename T >
T* find max( T* array, size t n )
  if ( n == 0 ) return NULL;
  T* result = &array[0];
  for ( size t i = 1; i < n; i++ ) {</pre>
    if ( array[i] > *result )
      result = &array[i];
  return result;
```

**Boolean Logic Gates for Adder** 

# **Core Computer Engineering Curriculum**

**Application Algorithm** Programming Language Computer Engineering **Operating System** Compiler Instruction Set Architecture Microarchitecture Register-Transfer Level Gate Level Circuits Devices Technology

ECE 2400 Computer Systems Programming

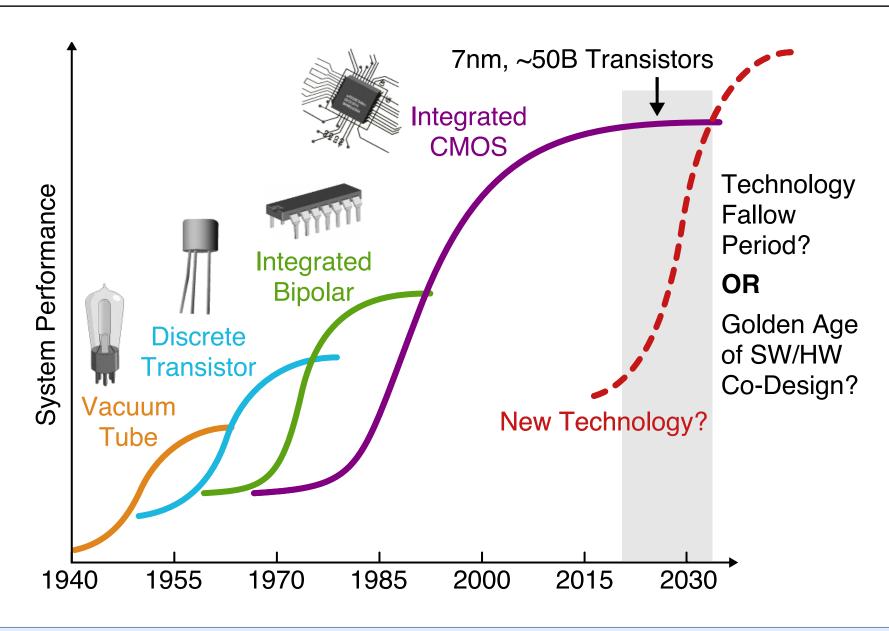
ECE 3140 Embedded Systems

ECE 4760 Design with Microcontrollers

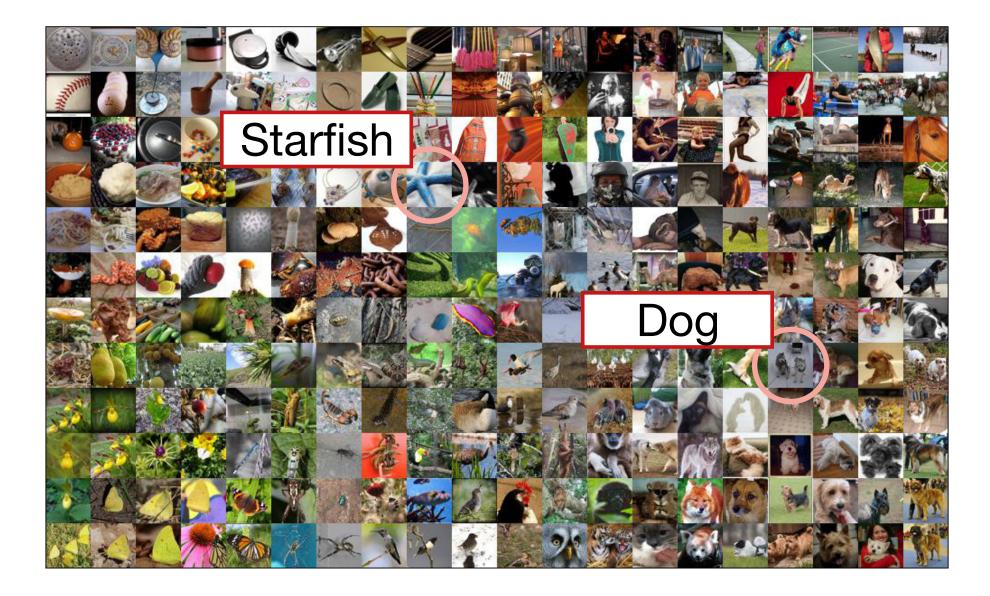
ECE 4750 Computer Architecture

ECE 2300 Digital Logic & Computer Org

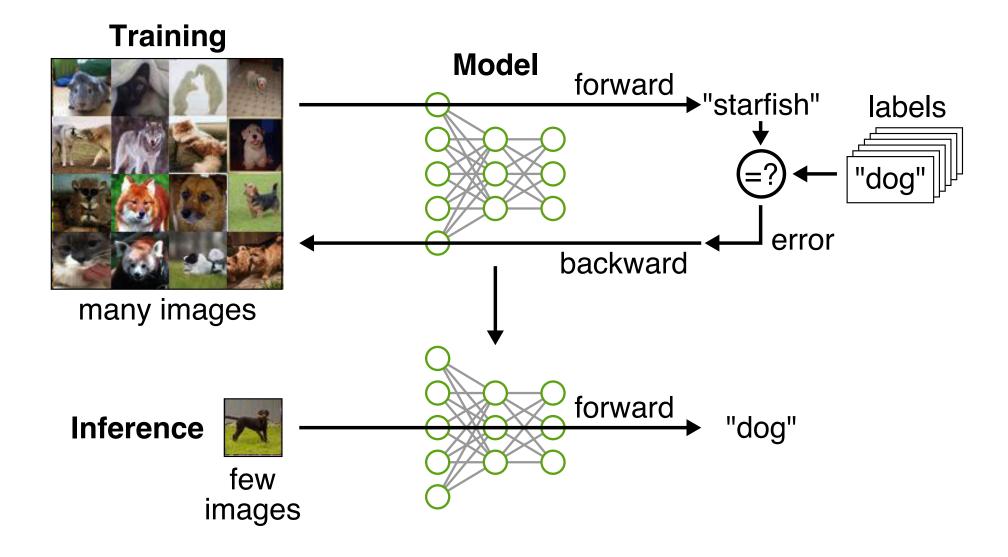
## **Technology Scaling is Slowing**



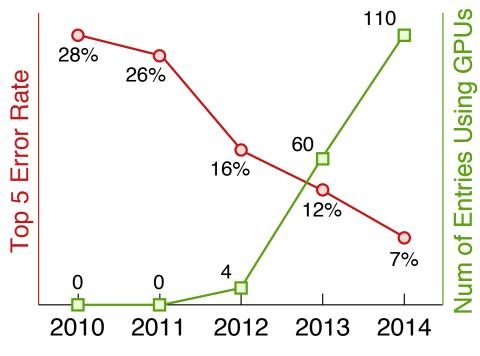
# **Example Application Domain: Image Recognition**

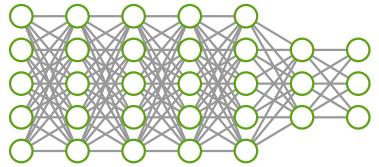


## Machine Learning: Training vs. Inference



# ImageNet Large-Scale Visual Recognition Challenge





Software: Deep Neural Network



**Hardware:** Graphics Processing Units



# SW/HW Co-Design for Deep Learning

Trends in Computer Engineering





Google TPU

## **Microsoft Catapult**

## **NVIDIA DGX-1**

- Graphics processor specialized just for machine learning
- Available as part of a complete system with both the software and hardware designed by **NVIDIA**
- Custom chip specifically designed to accelerate Google's TensorFlow C++ library
- Tightly integrated into Google's data centers
- ► 15–30× faster than contemporary CPU and **GPUs**

- Custom FPGA board for accelerating Bing search and machine learning
- Accelerators developed with/by app developers
- Tightly integrated into Microsoft data center's and cloud computing platforms

# SW/HW Co-Design Across Computing Spectrum

### **Cloud Computing**



## **Autonomous Driving**



## **Wearable Computing**

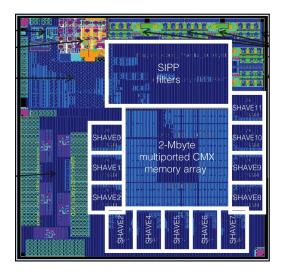




Google Cloud TPU



**NVIDIA** Drive PX2



Movidius Myriad 2

The field of computer engineering is experiencing a disruptive sea change and has a critical choice:

- 1. A technological fallow period
- 2. A golden age of SW/HW co-design

Majoring in electrical and computer engineering means you will have the opportunity to shape this golden age!

## **Build Software/Hardware for IoT Startups**

## **Particle: Photon**

WiFi

connected µcontrollers

w/

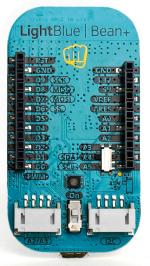
Particle Cloud

Punch Through













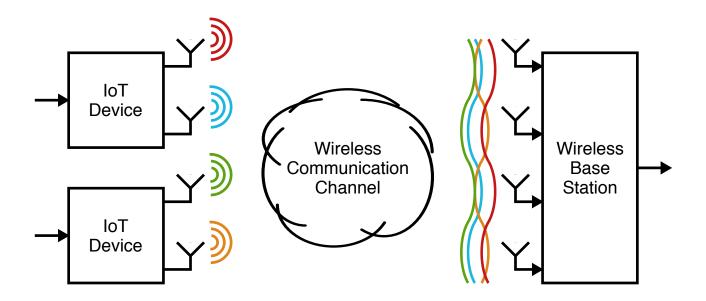


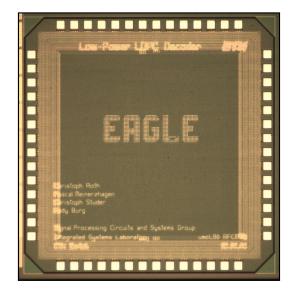
Devices Particle Cloud

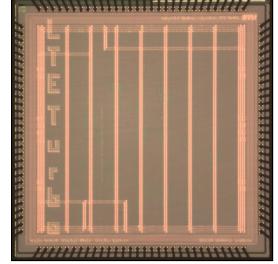


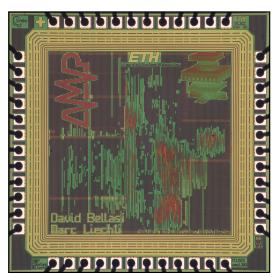
**Applications** 

## **Develop Algorithms and Chips for IoT**



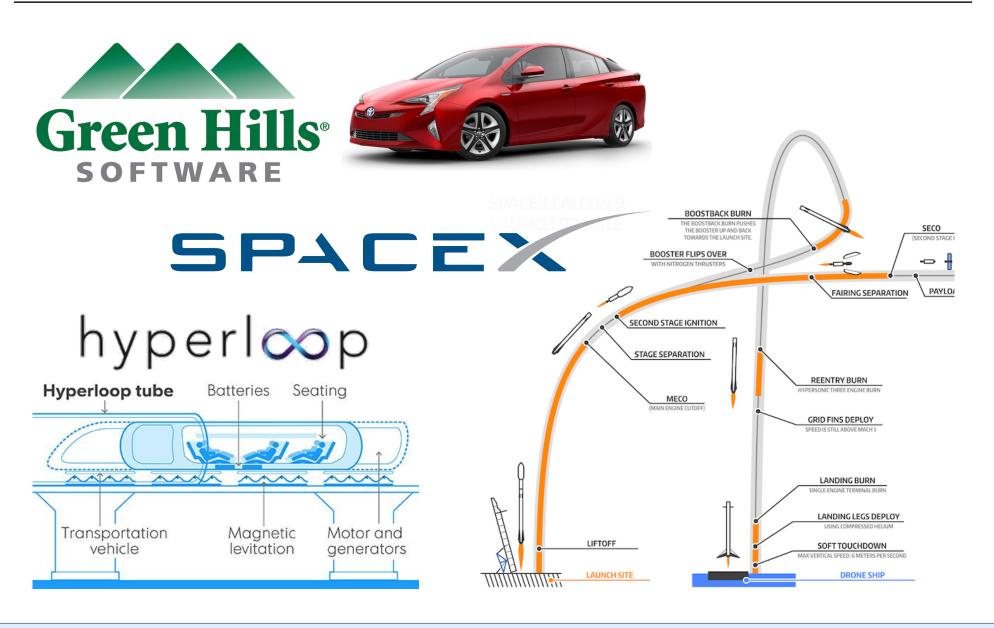






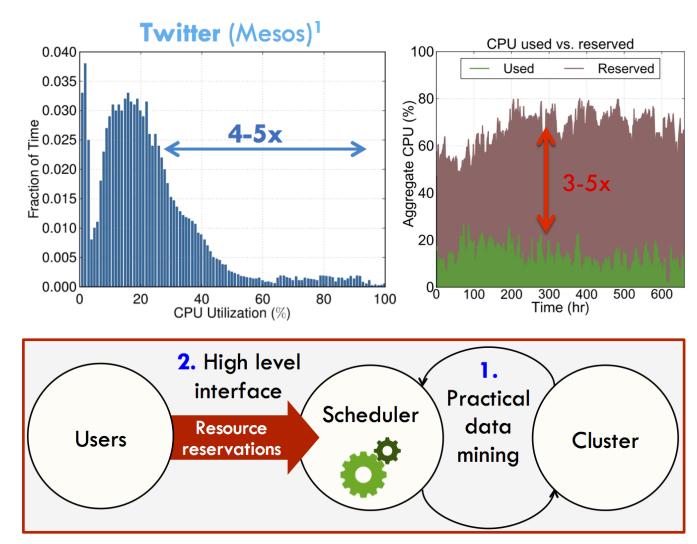
Research from Prof. Christoph Studer, ECE @ Cornell University

## **Develop Embedded Software and Gateware**



## **Build System-Level Software for Data Centers**





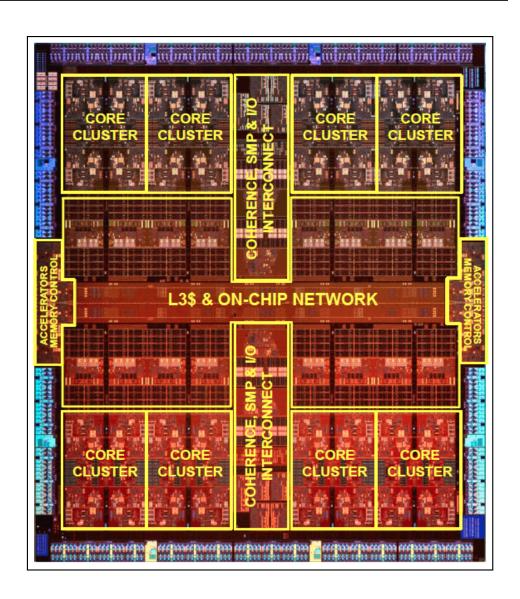
Paragon [ASPLOS'13,TopPicks'14] Quasar [ASPLOS'14]

Research by Prof. Christina Delimitrou, ECE @ Cornell University

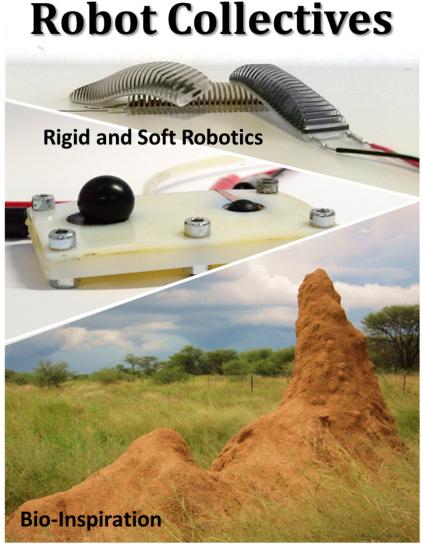
# **Build High-Performance Chips for Data Centers**

## **Oracle's Sparc M7 Processor**

- ► 4+ GHz in TSMC 16 nm
- 10B transistors
- 32 cores 256 threads per chip
- On-chip 64MB L3 cache
- Specialized hardware accelerators
  - Solaris Operating System
  - Java middleware
  - Oracle's relational database



## **Build Software/Hardware for Robotics**





Research from Prof. Kirstin Pretersen, ECE @ Cornell University