

# David H. Albonesi

School of Electrical and Computer Engineering  
333 Rhodes Hall, Cornell University  
Ithaca, NY 14853  
(607) 254-5473  
albonesi@csl.cornell.edu

## Education

2/92-9/96 Doctor of Philosophy, Computer Engineering, University of Massachusetts Amherst

1/83-5/86 Master of Science, Electrical Engineering, Syracuse University

9/78-5/82 Bachelor of Science, Electrical Engineering, University of Massachusetts Amherst

## Professional Experience

7/04- Associate Professor, Electrical and Computer Engineering, Cornell University  
Research and teaching in high performance, power efficient, and reliability-aware computer architecture.

7/04- Adjunct Associate Professor, Electrical and Computer Engineering, University of Rochester

6/01-6/04 Associate Professor, Electrical and Computer Engineering, University of Rochester

7/96-5/01 Assistant Professor, Electrical and Computer Engineering, University of Rochester

6/93-6/96 Research Engineer, Electrical and Computer Engineering, University of Massachusetts  
Digital systems consulting, system administration, and evaluation of architectural organizations and benchmark performance of supercomputers and workstations.

1/92-6/95 Lecturer, Electrical and Computer Engineering, University of Massachusetts  
Revamped undergraduate computer systems and microprocessor design laboratory courses to include design considerations and debugging techniques for high-volume manufacturing.

5/86-9/92 Section Manager/Principal Engineer, Processor Development, Prime Computer, Inc.  
Project manager and computer architect for high performance uniprocessor and multiprocessor memory hierarchy and system interconnect designs, implemented using CMOS and ECL technologies.

7/82-5/86 Senior Associate Engineer, Memory Development, IBM Corporation  
IBM 3090 mainframe main memory subsystem development including chip design and verification, circuit and board-level analysis, and hardware prototype debugging and integration with other subsystems.

## Honors and Awards

IEEE Micro Top Picks in Microarchitecture (2006, 2003)

IBM Faculty Award (2003, 2002, 2001)

NSF CAREER Award (1997)

Prime Computer Patent Plateau Award (1990)

Two Prime Computer Excellence Awards (1988, 1990)

IBM Excellence Award (1984)

## Memberships

Senior Member: IEEE Computer Society

Member: ACM SIGARCH

Member: Center for Electronic Imaging Systems

Member: Graduate Fields of ECE and CS, Cornell University

Member: Tau Beta Pi and Eta Kappa Nu

## Book Chapters

“Alleviating Thermal Constraints while Maintaining Performance Via Silicon-Based On-Chip Optical Interconnects,” N. Nelson, G. Briggs, M. Haurylau, G. Chen, H. Chen, D.H. Albonesi, E.G. Friedman, and P.M. Fauchet, *Unique Chips and Systems*, CRC Press, 2007.

“Power-Efficient Issue Queue Design,” A. Buyuktosunoglu, D.H. Albonesi, S. Schuster, D. Brooks, P. Bose, P. Cook, in *Power Aware Computing*, R. Graybill and R. Melhem (Eds), Kluwer Academic Publishers, Chapter 3, pp. 37-60, 2002.

“Low-Voltage 0.25um CMOS Improved Power Adaptive Issue Queue For Embedded Microprocessors,” B. Curran, M. Gifaldi, J. Martin, A. Buyuktosunoglu, M. Margala, D. Albonesi, in *SOC Design Methodologies*, M. Robert, B. Rouzeyre, C. Piguet, and M.-L. Flottes (Eds), Kluwer Academic Publishers, pp. 289-300, 2002.

## Journal Publications

“Addressing Thermal Non-Uniformity in SMT Workloads,” J.A. Winter and D.H. Albonesi, *ACM Transactions on Architecture and Code Optimization*, Vol. 5, No. 1, May 2008.

“On-chip Optical Technology in Future Bus-based Multicore Designs: Opportunities and Challenges,” N. Kirman, M. Kirman, R.K. Dokania, J. Martínez, A.B. Apsel, M.A. Watkins, and D.H. Albonesi, *IEEE Micro*, Special Issue on the Top Picks from Microarchitecture Conferences, January/February 2007.

“On-Chip Optical Interconnect Roadmap: Challenges and Critical Directions,” M. Haurylau, G. Chen, H. Chen, J. Zhang, N.A. Nelson, D.H. Albonesi, E.G. Friedman, and P.M. Fauchet, *IEEE Journal of Selected Topics in Quantum Electronics*, Special Issue on silicon Photonics, Vol. 12, No. 6, pp. 1699-1705, November/December 2006.

“Power Efficient Error Tolerance in Chip Multi-Processors,” M.W. Rashid, E.J. Tan, M.C. Huang, and D.H. Albonesi, *IEEE Micro*, Special Issue on Reliability-Aware Microarchitectures, Vol. 25, No. 6, pp. 60-70, November/December 2005.

“Micro’s Top Picks from Microarchitecture Conferences,” D.H. Albonesi, *IEEE Micro*, Guest Editor’s Introduction for Special Issue on Micro’s Top Picks from Microarchitecture Conferences, Vol. 24, No. 6, pp. 8-9, November/December 2004.

“An Evaluation of a Configurable VLIW Microarchitecture for Embedded DSP Applications,” W. Liu, D.H. Albonesi, J. Gostomski, L. Palum, D. Hinterberger, R. Wanzienried, and M. Indovina, *Journal of Circuits, Systems, and Computers*, Special Issue on VLSI Architectures for Multimedia Applications, Vol. 13, No. 6, pp. 1321-1345, December 2004.

“Dynamically Tuning Processor Resources with Adaptive Processing,” D.H. Albonesi, R. Balasubramonian, S.G. Dropsho, S. Dwarkadas, E.G. Friedman, M.C. Huang, V. Kursun, G. Magklis, M.L. Scott, G. Semeraro, P. Bose, A. Buyuktosunoglu, P.W. Cook, and S.E. Schuster, *IEEE Computer*, Special Issue on Power-Aware Computing, Vol. 36, No. 12, pp. 49-58, December 2003.

“Dynamic Frequency and Voltage Scaling for a Multiple-Clock-Domain Microprocessor,” G. Magklis, G. Semeraro, D.H. Albonesi, S.G. Dropsho, S. Dwarkadas, and M.L. Scott, *IEEE Micro*, Special Issue on the Top Picks from Microarchitecture Conferences, Vol. 23, No. 6, pp. 62-68, November/December 2003.

“A Dynamically Tunable Memory Hierarchy,” R. Balasubramonian, D.H. Albonesi, A. Buyuktosunoglu, and S. Dwarkadas, *IEEE Transactions on Computers*, Vol. 52, No. 10, pp. 1243-1258, October 2003.

“Power and Complexity Aware Design,” P. Bose, D.H. Albonesi, and D. Marculescu, *IEEE Micro*, Guest Editors’ Introduction for Special Issue on Power and Complexity Aware Design, Vol. 23, No. 5, pp. 8-11, September/October 2003.

“Selective Cache Ways: On-Demand Cache Resource Allocation,” D.H. Albonesi, *Journal of Instruction-Level Parallelism*, Special Issue on the Best Papers from the 32nd International Symposium on Microarchitecture, Vol. 2, 2000.

“Runtime Reconfiguration Techniques for Efficient General Purpose Computation,” B. Xu and D.H. Albonesi, *IEEE Design & Test of Computers*, Special Issue on Configurable Computing, pp. 42-52, January-March, 2000.

“STATS: A Framework for Microprocessor and System-Level Design Space Exploration,” D.H. Albonesi and I. Koren, *Journal of Systems Architecture*, Special Issue on Microprocessor Architecture, Vol. 45, No. 12-13, pp. 1097-1110, June 1999.

“A Mean Value Analysis Multiprocessor Model Incorporating Superscalar Processors and Latency Tolerating Techniques,” D.H. Albonesi and I. Koren, *International Journal of Parallel Programming*, Special Issue on Parallel Architectures and Compilation Techniques, Vol. 24, No. 3, pp. 235-263, August 1996.

## Refereed Conference and Workshop Publications

“Shared Reconfigurable Architectures for CMPs,” M.A. Watkins, M.J. Cianchetti, and D.H. Albonesi, *18th IEEE International Conference on Field Programmable Logic and Applications*, September 2008.

“The Scalability of Scheduling Algorithms for Unpredictably Heterogeneous CMP Architectures,” J.A. Winter and D.H. Albonesi, *Workshop on Parallel Execution of Sequential Programs on Multi-core Architectures*, held at the *35th International Symposium on Computer Architecture*, June 2008.

“Scheduling Algorithms for Unpredictably Heterogeneous CMP Architectures,” J.A. Winter and D.H. Albonesi, *38th International Conference on Dependable Systems and Networks*, June 2008.

“On-Chip Optical Interconnects: Challenges and Critical Directions,” G. Chen, H. Chen, M. Haurylau, N.A. Nelson, D.H. Albonesi, P.M. Fauchet, and E.G. Friedman, *Proceedings of the European Optical Society Topical Meeting on Optical Microsystems*, p. 97, October 2007.

“On-Chip Optical Interconnect for Reduced Delay Uncertainty,” G. Chen, H. Chen, M. Haurylau, N.A. Nelson, D.H. Albonesi, P.M. Fauchet, and E.G. Friedman, *Proceedings of Nano-Net*, September 2007.

“Dynamic Capacity-Speed Tradeoffs in SMT Processor Caches,” S. Lopez, S. Dropsho, D.H. Albonesi, O. Garnica, and J. Lanchares, *International Conference on High Performance Embedded Architectures and Compilers*, January 2007.

“Leveraging Optical Technology in Future Bus-based Chip Multiprocessors,” N. Kirman, M. Kirman, R.K. Dokania, J. Martínez, A.B. Apsel, M.A. Watkins, and D.H. Albonesi, *39th International Symposium on Microarchitecture*, December 2006.

“Synergistic Temperature and Energy Management in GALS Processor Architectures,” Y. Zhu and D.H. Albonesi, *International Symposium on Low Power Electronics and Design*, pp. 55-60, October 2006.

“On-Chip Copper-Based vs. Optical Interconnects: Delay Uncertainty, Latency, Power, and Bandwidth Density Comparative Predictions,” G. Chen, H. Chen, M. Haurylau, N.A. Nelson, D.H. Albonesi, P.M. Fauchet, and E.G. Friedman, *IEEE International Interconnect Technology Conference*, pp. 39-41, June 2006.

“Localized Microarchitecture-Level Voltage Management,” Y. Zhu and D.H. Albonesi, *International Symposium on Circuits and Systems*, pp. 37-40, May 2006.

“Compatible Phase Co-Scheduling on a CMP of Multi-Threaded Processors,” A. El-Moursy, R. Garg, D.H. Albonesi, and S. Dwarkadas, *20th International Parallel and Distributed Processing Symposium*, April 2006.

“Exploiting Coarse-Grain Verification Parallelism for Power-Efficient Fault Tolerance,” M.W. Rashid, E.J. Tan, M.C. Huang, and D.H. Albonesi, *14th International Conference on Parallel Architectures and Compilation Techniques*, pp. 315-325, September 2005.

“On-chip Optical Interconnect Roadmap: Challenges and Critical Directions,” M. Haurylau, H. Chen, J. Zhang, G. Chen, N.A. Nelson, D.H. Albonesi, E.G. Friedman, and P.M. Fauchet, *2nd International Group IV Photonics Conference*, pp. 17-19, September 2005.

“QUILT: A GUI-based Integrated Circuit Floorplanning Environment for Computer Architecture Research and Education,” G.J. Briggs, E.J. Tan, N.A. Nelson, and D.H. Albonesi, *Workshop on Computer Architecture Education*, June 2005.

“Electrical and Optical On-Chip Interconnects in Scaled Microprocessors,” G. Chen, H. Chen, M. Haurylau, N. Nelson, D.H. Albonesi, P.M. Fauchet, and E.G. Friedman, *International Symposium on Circuits and Systems*, pp. 2514-2517, May 2005.

“Predictions of CMOS Compatible On-Chip Optical Interconnect,” G. Chen, H. Chen, M. Haurylau, N. Nelson, P.M. Fauchet, E.G. Friedman, and D.H. Albonesi, *7th International Workshop on System Level Interconnect Prediction*, pp. 13-20, April 2005.

“A High Performance, Energy Efficient, GALS Processor Microarchitecture with Reduced Implementation Complexity,” Y. Zhu, D.H. Albonesi, and A. Buyuktosunoglu, *International Symposium on Performance Analysis of Systems and Software*, pp. 42-53, March 2005.

“Partitioning Multi-Threaded Processors with a Large Number of Threads,” A. El-Moursy, R. Garg, D.H. Albonesi, and S. Dwarkadas, *International Symposium on Performance Analysis of Systems and Software*, pp. 112-123, March 2005.

“Alleviating Thermal Constraints while Maintaining Performance Via Silicon-Based On-Chip Optical Interconnects,” N. Nelson, G. Briggs, M. Haurylau, G. Chen, H. Chen, D.H. Albonesi, E.G. Friedman, and P.M. Fauchet, *Workshop on Unique Chips and Systems*, March 2005.

“Dynamically Trading Frequency for Complexity in a GALS Microprocessor,” S. Dropsho, G. Semeraro, D.H. Albonesi, G. Magklis, and M.L. Scott, *37th International Symposium on Microarchitecture*, pp. 157-168, December 2004.

“Dynamically Matching ILP Characteristics Via a Heterogeneous Clustered Microarchitecture,” L. Chen, D.H. Albonesi, and S. Dropsho, *IBM Watson Conference on the Interaction Between Architecture, Circuits, and Compilers*, pp. 136-143, October 2004.

“The Energy Impact of Aggressive Loop Fusion,” Y. Zhu, G. Magklis, M.L. Scott, C. Ding, and D.H. Albonesi, *13th International Conference on Parallel Architectures and Compilation Techniques*, pp. 153-164, September 2004.

“Mitigating Inductive Noise in SMT Processors,” W. El-Essawy and D.H. Albonesi, *International Symposium on Low Power Electronics and Design*, pp. 332-337, August 2004.

“Hiding Synchronization Delays in a GALS Processor Microarchitecture,” G. Semeraro, D.H. Albonesi, G. Magklis, M.L. Scott, S.G. Dropsho, and S. Dwarkadas, *10th International Symposium on Asynchronous Circuits and Systems*, pp. 159-169, April 2004.

“Improving Application Performance by Dynamically Balancing Speed and Complexity in a GALS Microprocessor,” G. Semeraro, D.H. Albonesi, S. Dropsho, G. Magklis, S.

Dwarkadas, and M.L. Scott, *Workshop on Application Specific Processors*, December 2003.

“Energy Efficient Co-Adaptive Instruction Fetch and Issue,” A. Buyuktosunoglu, T. Karkhanis, D.H. Albonesi, and P. Bose, *30th International Symposium on Computer Architecture*, pp. 147-156, June 2003.

“Dynamically Managing the Communication-Parallelism Trade-off in Future Clustered Processors,” R. Balasubramonian, S. Dwarkadas, and D.H. Albonesi, *30th International Symposium on Computer Architecture*, pp. 275-286, June 2003.

“Profile-based Dynamic Voltage and Frequency Scaling for a Multiple Clock Domain Microprocessor,” G. Magklis, M.L. Scott, G. Semeraro, D.H. Albonesi, and S. Dropsho, *30th International Symposium on Computer Architecture*, pp. 14-25, June 2003.

“Front-End Policies for Improved Issue Efficiency in SMT Processors,” A. El-Moursy and D.H. Albonesi, *9th International Symposium on High-Performance Computer Architecture*, pp. 31-40, February 2003.

“Dynamic Data Dependence Tracking and its Application to Branch Prediction,” L. Chen, S. Dropsho, and D.H. Albonesi, *9th International Symposium on High-Performance Computer Architecture*, pp. 65-76, February 2003.

“Dynamic Frequency and Voltage Control for a Multiple Clock Domain Microarchitecture,” G. Semeraro, D.H. Albonesi, S.G. Dropsho, G. Magklis, S. Dwarkadas, and M.L. Scott, *35th International Symposium on Microarchitecture*, pp. 356-367, November 2002.

“Managing Static Leakage Energy in Microprocessor Functional Units,” S. Dropsho, V. Kursun, D.H. Albonesi, S. Dwarkadas, and E.G. Friedman, *35th International Symposium on Microarchitecture*, pp. 321-332, November 2002.

“Integrating Adaptive On-Chip Storage Structures for Reduced Dynamic Power,” S. Dropsho, A. Buyuktosunoglu, R. Balasubramonian, D.H. Albonesi, S. Dwarkadas, G. Semeraro, G. Magklis, and M.L. Scott, *11th International Conference on Parallel Architectures and Compilation Techniques*, pp. 141-152, September 2002.

“An Oldest-First Selection Logic Implementation for Non-Compacting Issue Queues,” A. Buyuktosunoglu, A. El-Moursy, and D.H. Albonesi, *15th International ASIC/SOC Conference*, pp. 31-35, September 2002.

“Tradeoffs in Power-Efficient Issue Queue Design,” A. Buyuktosunoglu, D.H. Albonesi, P. Bose, P. Cook, S. Schuster, *International Symposium on Low Power Electronics and Design*, pp. 184-189, August 2002.

“A Microarchitectural-Level Step-Power Analysis Tool,” W. El-Essawy, D.H. Albonesi, and B. Sinharoy, *International Symposium on Low Power Electronics and Design*, pp. 263-266, August 2002.

“Energy Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling,” G. Semeraro, G. Magklis, R. Balasubramonian, D.H. Albonesi, S. Dwarkadas, and M.L. Scott, *8th International Symposium on High-Performance Computer Architecture*, pp. 29-40, February 2002.

- “Early Stage Definition of LPX: A Low Power Issue-Execute Processor,” P. Bose, D. Brooks, A. Buyuktosunoglu, P. Cook, K. Das, P. Emma, M. Gschwind, H. Jacobson, T. Karkhanis, P. Kudva, S. Schuster, J. Smith, V. Srinivasan, V. Zyuban, D. Albonesi, S. Dwarkadas, *Workshop on Power-Aware Computer Systems*, February 2002.
- “Reducing the Complexity of the Register File in Dynamic Superscalar Processors , R. Balasubramonian, S. Dwarkadas, and D.H. Albonesi, *34th International Symposium on Microarchitecture*, pp. 237-248, December 2001.
- “A Dynamic Reconfigurable Clock Generator , R.M. Secareanu, D. Albonesi, and E.G. Friedman, *14th International ASIC/SOC Conference*, pp. 330-333, September 2001.
- “Dynamically Allocating Processor Resources Between Nearby and Distant ILP , R. Balasubramonian, S. Dwarkadas, and D.H. Albonesi, *28th International Symposium on Computer Architecture*, pp. 26-37, June 2001.
- “A Circuit Level Implementation of an Adaptive Issue Queue for Power-Aware Microprocessors,” A. Buyuktosunoglu, S. Schuster, D. Brooks, P. Bose, P. Cook, and D.H. Albonesi, *11th Great Lakes Symposium on VLSI*, pp. 73-78, March 2001.
- “Memory Hierarchy Reconfiguration for Energy and Performance in General Purpose Processor Architectures,” R. Balasubramonian, D.H. Albonesi, A. Buyuktosunoglu, and S. Dwarkadas, *33rd International Symposium on Microarchitecture*, pp. 245-257, December 2000.
- “An Adaptive Issue Queue for Reduced Power at High Performance,” A. Buyuktosunoglu, S. Schuster, D. Brooks, P. Bose, P. Cook, and D.H. Albonesi, *Workshop on Power-Aware Computer Systems*, November 2000.
- “Dynamic Memory Hierarchy Performance Optimization,” R. Balasubramonian, D.H. Albonesi, A. Buyuktosunoglu, and S. Dwarkadas, *Workshop on Solving the Memory Wall Problem*, June 2000.
- “An Architectural and Circuit-Level Approach to Improving the Energy Efficiency of Microprocessor Memory Structures,” D.H. Albonesi, *10th International Conference on VLSI*, pp. 192-203, December 1999.
- “Selective Cache Ways: On-Demand Cache Resource Allocation,” D.H. Albonesi, *32nd International Symposium on Microarchitecture*, pp. 248-259, November 1999.
- “A Methodology for the Analysis of Dynamic Application Parallelism and Its Application to Reconfigurable Computing,” B. Xu and D.H. Albonesi, *SPIE International Conference on Reconfigurable Technology: FPGAs for Computing and Applications*, pp. 78-86, September 1999.
- “Dynamic IPC/Clock Rate Optimization,” D.H. Albonesi, *25th International Symposium on Computer Architecture*, pp. 282-292, June 1998.
- “The Inherent Energy Efficiency of Complexity-Adaptive Processors,” D.H. Albonesi, *Power-Driven Microarchitecture Workshop*, pp. 107-112, June 1998.
- “Improving the Memory Bandwidth of Highly-Integrated, Wide-Issue, Microprocessor-Based Systems,” D.H. Albonesi and I. Koren, *5th International Conference on Parallel Architectures and Compilation Techniques*, pp. 126-135, November 1997.

“An Automated and Flexible Framework for Integrated Microprocessor and System-Level Design Space Exploration,” D.H. Albonesi and I. Koren, *Workshop on Performance Analysis and its Impact on Design*, pp. 25-34, June 1997.

“Architecture and Technology Tradeoffs in the Design of Next-Generation Multiprocessor Servers,” D.H. Albonesi and I. Koren, *7th IEEE Symposium on Parallel and Distributed Processing*, pp. 174-181, October 1995.

“An Analytical Model Of High Performance Superscalar-Based Multiprocessors,” D.H. Albonesi and I. Koren, *3rd International Conference on Parallel Architectures and Compilation Techniques*, pp. 194-203, June 1995.

“Tradeoffs in the Design of Single Chip Multiprocessors,” D.H. Albonesi and I. Koren, *2nd International Conference on Parallel Architectures and Compilation Techniques*, pp. 25-34, August 1994.

### **Patents Issued and Pending**

“Multiple Clock Domain Microprocessor,” D.H. Albonesi, G. Semeraro, G. Magklis, M.L. Scott, R. Balasubramonian, and S. Dwarkadas, U.S. Patent 7,089,443, issued 8/4/06.

“Memory Hierarchy Reconfiguration for Energy and Performance in General-Purpose Processor Architectures,” R. Balasubramonian, D.H. Albonesi, A. Buyuktosunoglu, and S. Dwarkadas, U.S. Patent 6,834,328, issued 12/21/04.

“Dynamically Reconfigurable Memory Hierarchy,” R. Balasubramonian, D.H. Albonesi, A. Buyuktosunoglu, and S. Dwarkadas, U.S. Patent 6,684,298, issued 1/27/04.

“Mechanism for Dynamically Altering the Complexity of a Microprocessor,” D.H. Albonesi, U.S. Patent 6,205,537, issued 3/20/01.

“Electric Cable Connection Error-Detect Method and Apparatus,” D.H. Albonesi, U.S. Patent 5,170,113, issued 12/8/92.

“Memory Board Selection Method and Apparatus,” D.H. Albonesi, U.S. Patent 5,119,486, issued 6/2/92.

“System Bus for Multiprocessor Computer System,” D.H. Albonesi, B.K. Langendorf, J. Chang, J.G. Faase, and M.J. Homberg, U.S. Patent 5,113,514, issued 5/12/92.

“Memory Error Correction System,” D.H. Albonesi, U.S. Patent 4,920,539, issued 4/24/90.

“Dynamically Managing the Communication-Parallelism Trade-off in Clustered Processors,” R. Balasubramonian, S. Dwarkadas, D.H. Albonesi, U.S. Patent filed, 6/05 (pending).

“Dynamic Data Dependence Tracking and Its Application to Branch Prediction,” L. Chen, S. Dropsho, D.H. Albonesi, U.S. Patent filed, 2/05 (pending).

“Method of Adaptive Control and Resizing of Issue Queue Structures Within an Out-of-order Superscalar Processor for Reduced Power at High Performance,” A. Buyuktosunoglu, S. Schuster, D. Brooks, P. Bose, P. Cook, and D.H. Albonesi, U.S. Patent filed, 10/01 (pending).

## **Graduated PhD Students**

Yongkang Zhu, “Hardware and Software Optimizations for Multiple Clock Domain Microprocessors,” Department of Electrical and Computer Engineering, University of Rochester, September 2005. First employment: Microsoft Corporation.

Ali El-Moursy, “Highly Efficient Multithreaded Architecture,” Department of Electrical and Computer Engineering, University of Rochester, August 2005 (unofficial co-advisor: Sandhya Dwarkadas). First employment: Intel Corporation.

Wael El-Essawy, “Architectural Level Analysis and Mitigation of Inductive Noise in Simultaneous Multi-Threaded Processors,” Department of Electrical and Computer Engineering, University of Rochester, October 2004. First employment: IBM Austin Research Laboratory.

Lei Chen, “Dynamic Data Dependence Tracking and its Applications,” Department of Electrical and Computer Engineering, University of Rochester, October 2004. First employment: IBM Austin Research Laboratory.

Greg Semeraro, “Multiple Clock Domain Microarchitecture Design and Analysis,” Department of Electrical and Computer Engineering, University of Rochester, October 2003. First employment: Rochester Institute of Technology.

Rajeev Balasubramonian, “Dynamic Management of Microprocessor Resources in Future Microprocessors,” Department of Computer Science, University of Rochester, August 2003 (unofficial co-advisor; advisor: Sandhya Dwarkadas). First employment: University of Utah.

Alper Buyuktosunoglu, “Power-Efficient Issue Queue Design,” Department of Electrical and Computer Engineering, University of Rochester, June 2003. First employment: IBM T.J. Watson Research Center.

## **Graduated MS Thesis Students**

Keith Kraft, “Trace Cache Hierarchies,” Department of Electrical and Computer Engineering, University of Rochester, May 2003. First employment: Intel Corporation.

## **Current PhD Students**

Jonathan Winter, Department of Computer Science, Cornell University.

Matt Watkins, School of Electrical and Computer Engineering, Cornell University.

Paula Petrica, School of Electrical and Computer Engineering, Cornell University (co-advised with Rajit Manohar).

Basit Sheikh, School of Electrical and Computer Engineering, Cornell University (co-advised with Rajit Manohar).

Mark Cianchetti, School of Electrical and Computer Engineering, Cornell University.

### **Former Undergraduate Research Students**

Greg Briggs (2005), Alvin Law (2002), Jethro Law (2000), John Strasser (1999), Department of Electrical and Computer Engineering, University of Rochester.

### **Current Undergraduate Research Students**

Joseph Kerekes, School of Electrical and Computer Engineering, Cornell University. Supported by a Semiconductor Research Corporation Education Alliance grant.

### **Former Postdoctoral Researcher**

Dr. Steven Dropsho, Department of Computer Science, University of Rochester, 9/2001-10/2003. Arrived after completing his PhD in Computer Science from the University of Massachusetts at Amherst. Employment: EPFL.

### **PhD Dissertation Committees**

- ECE Volkan Kursun, Magdy El-Moursy, Andrey Meshiba, Dimitrios Velenis, Kevin Tang, Tolga Soyata, Ivan Kourtev, Victor Adler (University of Rochester); Paruj Ratanaworabhan, Jian Li, Engin Ipek, Meyrem Kirman, Vince Weaver, David Biermann, Ramazan Bitirgen (Cornell); Jaume Abella (Universitat Politecnica de Catalunya [UPC]); Sonia Lopez (Universidad Complutense de Madrid).
- CS Yutao Zhong, Grigoris Magklis, Umit Rencuzogullari, Galen Hunt, Robert Stets (University of Rochester); Anne Bracy (University of Pennsylvania).

### **MS Thesis Committees**

- ECE Michael Wieckowski (University of Rochester).

### **Courses Developed and Taught**

#### *High Performance Microprocessor-Based Systems*

Graduate course that studies advanced research topics in high performance microarchitecture, and the microarchitecture of current industry designs.

#### *Contemporary Issues in Computer Architecture*

Graduate course covering research in high performance microarchitecture, with an emphasis on power and reliability.

#### *Advanced Computer Architecture*

Senior and graduate level computer architecture.

#### *Computer Organization*

Undergraduate level computer organization.

#### *Introduction to Digital Logic Design*

Undergraduate course in digital logic design.

#### *Computer Design Project*

Undergraduate design project course for students concentrating in computer engineering.

*Reconfigurable Microprocessor Design*

Graduate research-oriented course that served as a springboard for a new research effort.

*Engineering Seminar*

Introductory course for Engineering freshman.

*ECE Colloquium*

Graduate ECE Colloquium course. Co-taught with Sally McKee.

## **Professional Activities**

Editor-In-Chief: IEEE Micro (2007-present)

Associate Editor: ACM Transactions on Architecture and Compiler Optimizations (2005-present)

Associate Editor: Journal of Circuits, Systems, and Computers (1999-present)

Associate Editor: IEEE Micro (2004-2006)

Special Issue Guest Editor (with P. Bose and D. Marculescu): *Power and Complexity Aware Design*, IEEE Micro, September/October, 2003

Workshop Co-organizer: *Workshop on Quality-Aware Design*, held at the International Symposium on Computer Architecture (2008)

Workshop Co-organizer: *Workshop on Complexity-Effective Design*, held at the International Symposium on Computer Architecture (2000-2006)

Tutorial Co-organizer: *Tutorial on Partially Asynchronous Microprocessors*, held at the International Symposium on Computer Architecture (2003) and the International Symposium on Microarchitecture (2002)

Tutorial Co-organizer: *Tutorial on Minimally Clocked Microprocessor Design*, held at the International Conference on Supercomputing (2002)

Panelist: "Will Future Processors and the Target Market Still be Driven by Moore's Law?", held at Cool Chips VIII (2005)

General Chair: International Symposium on Performance Analysis of Systems and Software (2007)

Program Committee Chair: International Symposium on Performance Analysis of Systems and Software (2006)

Program Committee Chair: IEEE Micro Top Picks from Microarchitecture Conferences (2004)

Program Committee Member: International Symposium on High Performance Computer Architecture (2009, 2005, 2004)

Program Committee Member: International Conference on High Performance and Embedded Architectures and Compilers (2009)

Program Committee Member: International Symposium on Microarchitecture (2008, 2006, 2004)

Program Committee Member: Workshop on Chip Multiprocessor Memory Systems and Interconnects (2008)

Program Committee Member: International Symposium on Computer Architecture (2007, 2006, 2005, 2004)

Program Committee Member: IEEE Micro Top Picks from Microarchitecture Conferences (2007, 2006, 2005)

Program Committee Member: Reconfigurable and Adaptive Architecture Workshop (2006)

Program Committee Member: Workshop on Architectures for Gigascale Integration (2006)

Program Committee Member: International Workshop on Advanced Low Power Systems (2006)

Program Committee Member: International Symposium on High Performance Computer Architecture Special Session on Industrial Perspectives on Challenges for Next-Generation Computer Systems (2005)

Program Committee Member: International Symposium on Parallel Architectures and Compilation Techniques (2005, 1997)

Program Committee Member: International Symposium on Low Power Electronics and Design (2005)

Program Committee Member: International Symposium on Performance Analysis of Systems and Software (2005, 2003, 2001)

Program Committee Member: Workshop on Power-Aware Computing Systems (2004, 2003, 2002, 2000)

Program Committee Member: Workshop on Power Management for Real-Time and Embedded Systems (2001)

Program Committee Member: Workshop on Performance Analysis and its Impact on Design (1998)

Proposal Review Panelist: National Science Foundation CAREER, Computer Systems Architecture, and Embedded and Hybrid Systems programs

Proposal Reviewer: National Science Foundation Design Automation and Experimental Systems programs

Proposal Reviewer: California MICRO program

Book Reviewer: MIT Press

Book Reviewer: Cambridge University Press

Reviewer of numerous journal and conference papers each year

My research group generated problem sets for the 3rd edition of *Computer Organization and Design: The Hardware/Software Interface* by D. Patterson and J. Hennessy

My research group generated the Chapter 2 Alpha instruction set statistics for the 3rd edition of *Computer Architecture: A Quantitative Approach* by J. Hennessy and D. Patterson

### **University/Departmental Service (Cornell)**

- '08-'09 Faculty Advisory Board on Information Technology  
Teaching Excellence Institute Faculty Advisory Council  
Curriculum and Standards Committee  
Faculty Advisor (Class of '09)  
Faculty Mentor
- '07-'08 Faculty Advisory Board on Information Technology  
Teaching Excellence Institute Faculty Advisory Council  
Building Committee  
Faculty Advisor (Class of '09)  
Faculty Mentor
- '06-'07 Chair, Computer Engineering and Circuits Recruiting Committee  
Graduate Committee  
Nominating Committee  
Faculty Advisor (Class of '09)  
Faculty Mentor
- '05-'06 Chair, Computer Engineering and Circuits Recruiting Committee  
Graduate Committee  
Nominating Committee  
First-year Faculty Advisor (Class of '09)  
Faculty Mentor  
Co-organizer (with Sally McKee) of the ECE colloquium

### **University/Departmental Service (Rochester)**

- '03-'04 Chair, Graduate Admissions Committee  
Faculty Recruiting Committee  
Department Resource Committee  
Advisor, Class of '06  
Faculty Mentor
- '02-'03 Chair, Graduate Admissions Committee  
Department Resource Committee  
Advisor, Class of '06  
Faculty Mentor
- '01-'02 Faculty Senate Research Policy Committee

Chair, Graduate Admissions Committee  
Undergraduate Committee  
Faculty Recruiting Committee  
Advisor, Class of '06  
Faculty Mentor

'00-'01 Faculty Senate Research Policy Committee  
Graduate Admissions Committee  
Undergraduate Committee  
Faculty Recruiting Committee  
ECE Webmaster  
Advisor, Class of '01

'99-'00 Undergraduate Committee  
Faculty Recruiting Committee  
ECE Faculty Secretary  
ECE Webmaster  
Advisor, Class of '01  
Orientation Program Reviewer

'98-'99 Undergraduate Committee  
Faculty Recruiting Committee  
ECE Faculty Secretary  
ECE Webmaster  
Advisor, Class of '01

'97-'98 Graduate Admissions Committee  
ECE Faculty Secretary  
ECE Webmaster  
Advisor, Class of '01  
Orientation Program Reviewer

'96-'97 Graduate Admissions Committee  
ECE Faculty Secretary